Semi conductors

Semi conductors are materials whose electronic properties are intermediate between those of good conductors and Insulators. The resistivity of Semi conductors varies from 10^{-5} to 10^{+4} ohm-m as compared to the conductors and Insulators. There are semi conductors such as Germanium and silicon which belong to group IV of periodic table. The resistivity of a Semi conductor is a function of temperature. With increase of temperature, the resistivity decreases so the electrical conductivity increases. Hence the Semi conductors have negative temperature co-efficient of resistance. The Semi conductors are classified as

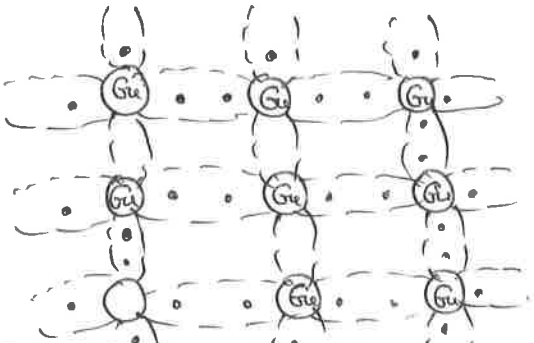
1) Intrinsic or pure Semi Conductor

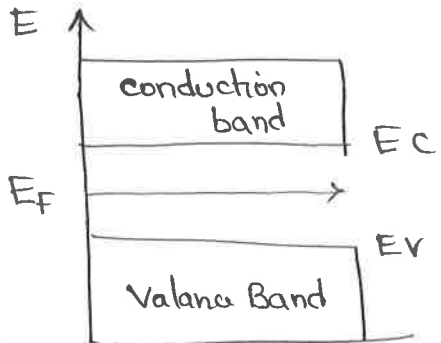
2) Extrinsic or Impure Semi Conductor

Intrinsic Semi conductor : It is a pure form of a semi conductor. In this semi conductor the number of Electrons are equal to the number of holes. The Electrical conductivity of this semi conductor solely determined by thermally generated carriers. Let us consider the case of Germanium (Ge) or Silicon (Si) $Si = 14 = 1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^2$

$Ge\ (32) = 1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^6\ 4s^2\ 3d^{10}\ 4p^2$

The valance electrons of Ge atom is shared with neighbouring atoms





However, with Increase of temperature few covalent bonds are broken. when a covalent bond is broken one electron becomes free and Leaves the atom and becomes positive ion known as hole. The hole acts as a positively charged particle having same charge as electron but opposite sign. This created hole attracts electron from neighbouring atom to fill it. Thus a hole once created moves in a random manner in the crystal. Thus the total semi conductor current is the combination of both hole and electron currents.

$$I_{total} = I_h + I_e$$

The Fermi Level E_F is at the middle of the valance and conduction bands.

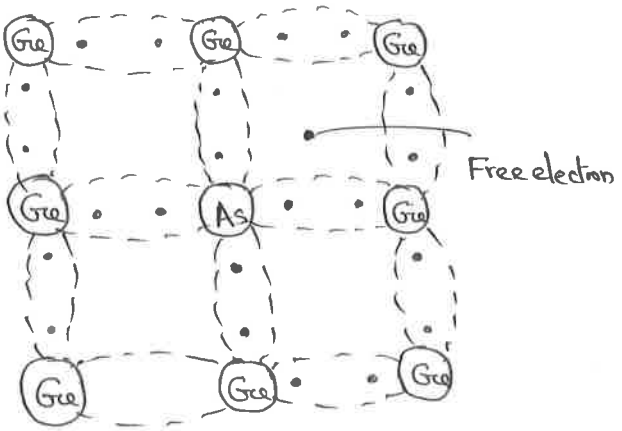
$$\therefore \quad E_F = \frac{E_c + E_v}{2}$$

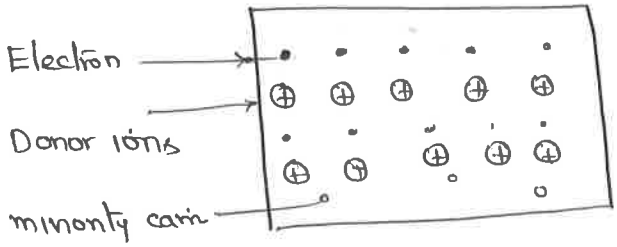
i.e the Fermi Level will be at the centre of two bands.

Extrinsic Semi Conductor :- of a small amount of impurity is added to a pure semi conductor it significantly changes the properties of the crystal like conductivity, resistivity, etc. The process of adding the Impurities to a semi conductor is known as doping. A semi conductor doped with Impurities is called Extrinsic Semi conductor. The Extrinsic semi conductors are further classified as

i) N type Semiconductor ii) P type Semi conductor.

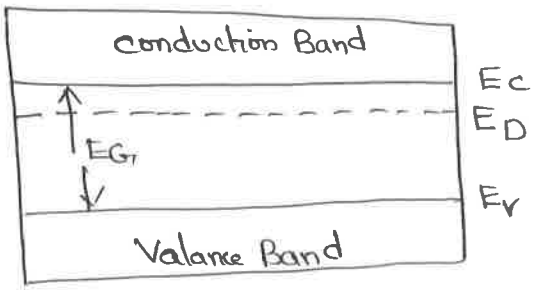
N-Type Semi conductor :- It is formed by adding pentavalent Impurities such as phosphorous, antimony and bismuth etc to intrinsic Semi conductor. This results in an additional electrons in the crystal. The electrons move away from the parent atom and the atoms get positive charges and they are known as Donor ions. The resultant Semiconductor of N type is given below.





N type Semi conductor

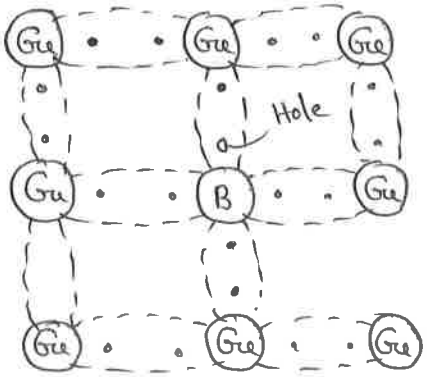
It should be noted that at room temperature almost all the fifth electrons of donor material are raised to the conduction Band.

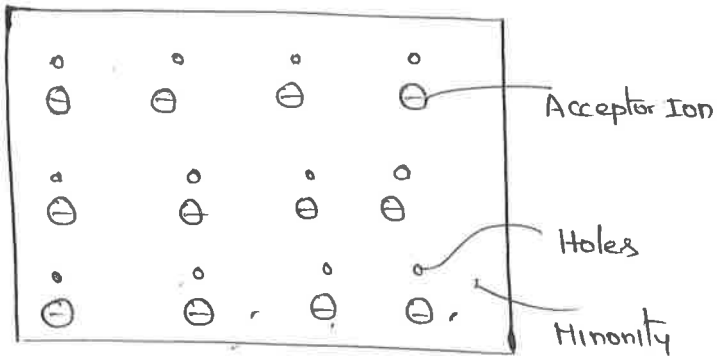


Energy Band diagram of N type.

If the intrinsic Semi conductor material is doped with n type impurities not only does the number of electrons increases but the no of holes decreases below the intrinsic value. The reason is due to increased rate of recombination of electrons with holes.

P-Type Semi Conductor :- when a small amount of trivalent impurity is added to a pure crystal the resulting crystal is called a Extrinsic Semiconductor of p type. Let us consider the case when trivalent atom boron is added to a pure Germanium crystal.



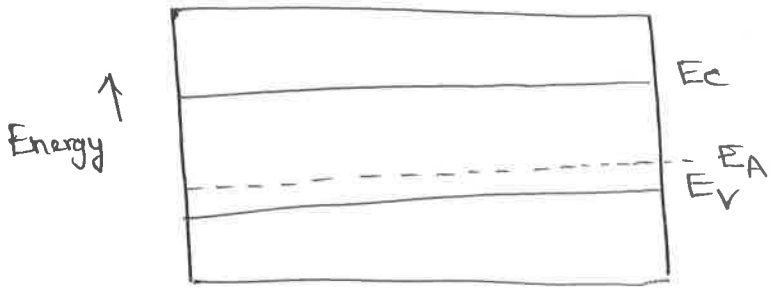


P- Type Semiconductor.

i) In p type semi conductors, holes are majority carriers and Electrons are minority carriers.

ii) The p type Semiconductor is electrically neutral as the no of mobile holes are equal to no of acceptors in all conditions

iii) when acceptor or P- type Impurities are added to the pure semiconductor they produce an allowble descrete energy level which is just above the valance band.



E.B of p type Semiconductor

Mass action Law :- Under thermal equilibrium the product of free negative and positive concentrations is constant independent of donor and acceptor impurity doping. This relationship is called the mass action law and is given by $np = n_i^2$ (The intrinsic concentration n_i is a function of temperature)

Charge densities in a Semi Conductor :-

Let N_D is the concentration of donor atoms and they are completely ionized then N_D positive charges per cubic meter are contributed by donor ions Hence total positive charge density is $N_D + p$. Similarly the total negative charge density is $N_A + n$.

Since the Semi conductor is Electrically neutral

$$N_D + p = N_A + n$$

i) For n type Material $N_A = 0$ and $n \gg p$ then

$$\boxed{N_D \approx n}$$

i.e in N type material the free electron concentration is approximately equal to the Density of donor atoms.

Using proper notation for material and mass action law for n type

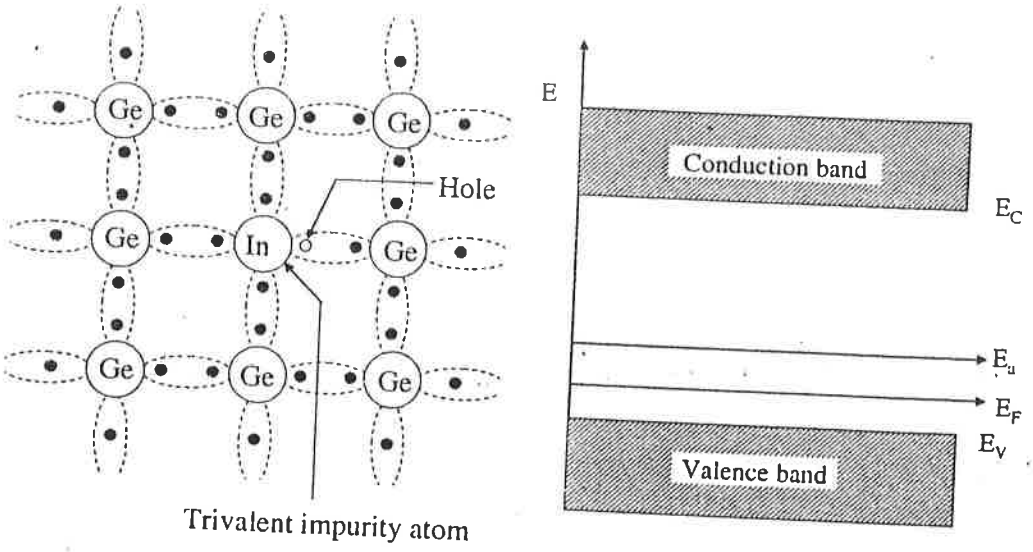
$$n_n p_n = n_i^2 \quad \text{but} \quad n_n \approx N_D$$

$$\therefore \boxed{p_n = \frac{n_i^2}{N_D}}$$

ii) For p type Material

$$n_p p_p = n_i^2 \qquad p_p \approx N_A$$

$$\boxed{n_p = \frac{n_i^2}{N_A}}$$



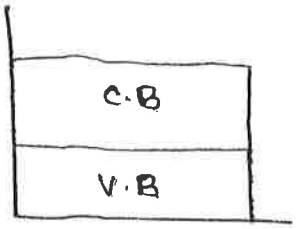
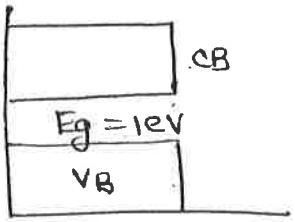
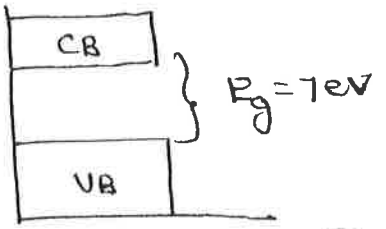
(a) Bond structure

(b) Energy band diagram

Fig. 16.3 Bond structure and energy band diagram of p-type semiconductor

An impurity that produces holes inside a semiconductor crystal is called acceptor impurity because it accepts electrons from the nearby germanium atoms. The semiconductor containing acceptor type of impurity is called p-type semiconductor, because the charge carriers are positive holes. The energy band diagram for p-type semiconductor is as shown in Fig. 16.3(b). Here E_a represents the energy level corresponding to the accepter impurities. When an intrinsic semiconductor is doped with accepter impurity, the concentration of holes in the valence band will be more than the concentration of electrons in conduction band and the Fermi level shifts towards the valence band. The accepter level is just above the valence band. It should be noted that in p-type semiconductors, holes are majority charge carriers and electrons are the minority charge carriers.

Distinction between Conductors, Semi Conductors and Insulators :-

Conductors	Semi Conductors	Insulators
Energy band diagram is 		
Conduction band and valance band overlap each other	Energy band gap is small compared to Insulator	Large gap exists between conduction band and valance band.
At room temperature conductivity is high.	conductivity is in between conductors and Insulators.	conductivity is zero.
Conductivity increases with increase of temperature.	conductivity decreases with increase of Temperature.	
It has positive temperature coefficient of resistance.	Semiconductors have negative temperature coefficient of resistance	
Example : Cu	Example : Ge, Si	Ex : Diamond
conductivity : 10^{-8} to 10^{-6} ohm-m	10^{-5} to 10^{4} ohm-m for Semiconductors.	10^{7} to 10^{8} ohm-m

Drift and Diffusion currents :-

Drift current

1. The current due to holes and electrons in a semi conductor in the presence of applied electric field is called as drift current. The average velocity attained by carriers is called as drift velocity.

2. Drift velocity V_d is proportional to applied electric field $\bar{E}$.

$$V_d \propto E$$

$$V_d = \mu E$$

Here μ = Mobility of Electrons

3. The current density $J = nev_d$

$$\boxed{J = ne\mu E}$$

4. Drift current due to electrons

$$J_n(\text{drift}) = ne\mu_n E$$

5. Drift current due to holes

$$J_p(\text{drift}) = pe\mu_p E$$

6. Total current (drift) : $J = \sigma E$

$$J = (n\mu_n + p\mu_p)eE$$

Diffusion current

1. It is the current due to diffusion carriers from high concentration to low concentration i.e it flows due concentration gradient.

2. The diffusion current is proportional to the concentration gradient.

$$J_n \propto \frac{dn}{dx}$$

$$J_n(\text{diffusion}) = eD_n\frac{dn}{dx}$$

$$J_p(\text{diffusion}) = -eD_p\frac{dp}{dx}$$

Here D_p, D_n are diffusion consts for holes and electrons.

$$J_{\text{diffusion}} = J_n + J_p$$

$$= -eD_p\frac{dp}{dx} + eD_n\frac{dn}{dx}$$

Note that hole and electron diffusion currents are in opposite directions in a semiconductor.

Total current In a Semiconductor :-

$$J = J_{drift} + J_{diffusion}$$

$$J = eE\left(n\mu_n + p\mu_p\right) - e D_p \frac{dp}{dx} + e D_n \frac{dn}{dx}$$

$$J = e\left[\left[n\mu_n E + D_n \frac{dn}{dx}\right] + \left[\left(p\mu_p E - D_p \frac{dp}{dx}\right)\right]\right]$$

Einestain's Equation :- The mobility of carriers expresses the ability of carriers to drift and diffusion const D expresses the ability of carriers to diffuse. Einestain relates the concepts of mobility and diffusion const D.

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{K_B T}{e}$$

Here D_n, D_p are diffusion constants for holes and electrons

μ_p, μ_n are Mobilities for holes and electrons.

According to Einestians Equation the ratio of diffusion const and Mobility is directly proportional to Absolute Temperature.

It also tells that D, μ increases with Temperature.

However, with increase of temperature, a few covalent bonds are broken. When a covalent bond is broken, one electron becomes free and leaves the atom and becomes a positive ion known as hole. The hole acts as a positively charged particle, having a charge equal to that of an electron but of opposite sign. Since a hole is a strong centre of attraction for the electron, the hole attracts an electron from the neighbouring atom to fill it. Thus the hole is now shifted to another place from where the electron has migrated. The newly created hole is filled up by another neighbouring electron and so on. Thus a hole once created moves about in the crystal in a random manner, just like the free electron. On applying an electric field, the holes move in a direction opposite to that of the valence electrons. It constitutes a hole current. It must be noted that in an intrinsic semiconductor, the number of electrons and holes are equal and they are less. Hence the current produced in a semiconductor is not adequate for any useful work. The energy band diagram of intrinsic semiconductor is shown in Fig. 16.1(b). The Fermi level E_F is at the middle of valence and conduction bands. If E_v and E_c are the energy levels of valence and conduction bands respectively, then the energy gap is,

$$E_g = E_c - E_v$$

and the Fermi energy is, $$E_F = \frac{E_c + E_v}{2}$$

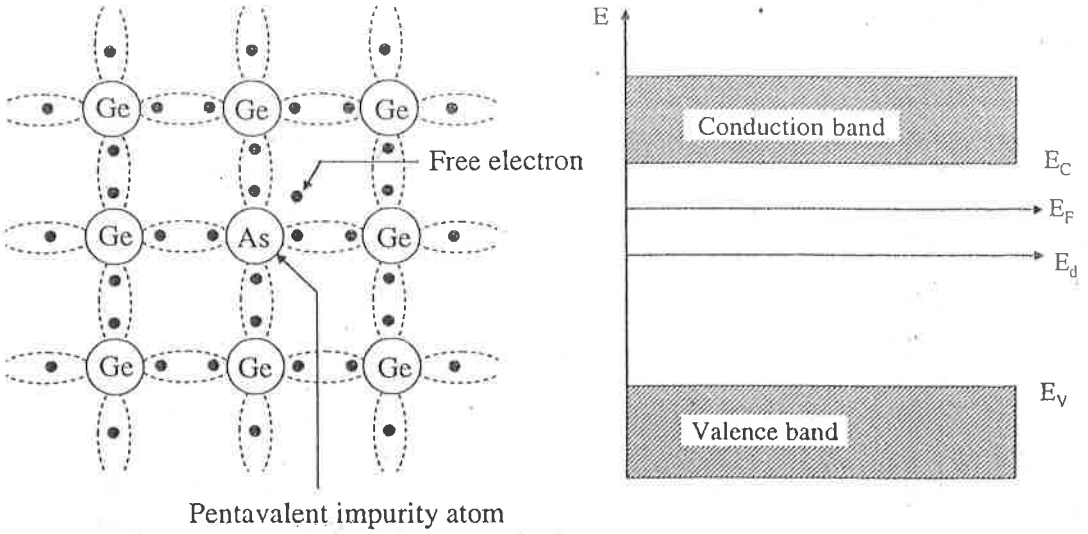
Extrinsic Semiconductors

If a small amount of impurity is added to a pure semiconductor, it significantly increases the conducting properties. The process of adding the impurities to a semiconductor is known as doping. A semiconductor doped with impurities is called extrinsic semiconductor. Depending upon the type of impurity added to pure semiconductors (like Ge or Si) the extrinsic semiconductors are further subdivided into two groups :

i) n-type semiconductor, ii) p-type semiconductor.

n-type semiconductor

A semiconductor doped with a pentavalent impurity is called n-type semiconductor. Typical examples of pentavalent impurities are arsenic (As, Z=33) and antimony (Sb, Z = 51). When these impurities are added to pure germanium crystal, four valence electrons of impurity atom form covalent bonds with the four valence electrons of the neighbouring Ge atoms. The fifth valence electron of impurity atom has no place to form the covalent bond and remains free to move randomly in the crystal lattice as shown in Fig.16.2(a). Thus each impurity atom donates a free electron to the semiconductor. Hence the impurity is called donor impurity. The semiconductor containing donor type impurity is called n-type semiconductor because it has negative charge carriers, i.e., electrons.



(a) Bond structure (b) Energy band diagram

Fig. 16.2 Bond structure and energy band diagram of n-type semiconductor

Although each arsenic atom donates one electron, yet doping the crystal with just a trace of impurity provides enough free electrons to move through the crystal structure and act as charge carrier. In the case of germanium, doped with donor impurities the energy required to move an electron from donor impurity to the conduction band is in the order of 0.0127 eV. The energy band diagram for n-type semiconductor is shown in Fig. 16.2(b). Here E_d represents the energy level corresponding to donor impurities and it lies just below the conduction band. It should be noted that in n-type semiconductors, the electrons are majority charge carriers but there are still present some thermally generated holes which are called the minority charge carriers.

p-type semiconductor

A semiconductor doped with a trivalent impurity is called p-type semiconductor. Typical examples of trivalent impurities are gallium (Ga, Z=31) and indium (In, Z=49). When a small amount of Indium is added to germanium crystal, three valence electrons of impurity atoms form covalent bonds with three valence electrons from three neighbouring germanium atoms. There is a deficiency of one electron to complete the fourth bond. This electron deficiency is called the hole and it behaves like a positively charged particle as shown in Fig. 16.3(a). Since there is a strong tendency of semiconductor crystal to form covalent bonds, a hole attracts one electron from a nearby covalent bond. Consequently a new hole is created at the originally occupied place of electron. This hole is again filled by another electron from a nearby bond giving rise to another hole and so on. Thus a hole moves freely throughout the crystal lattice.

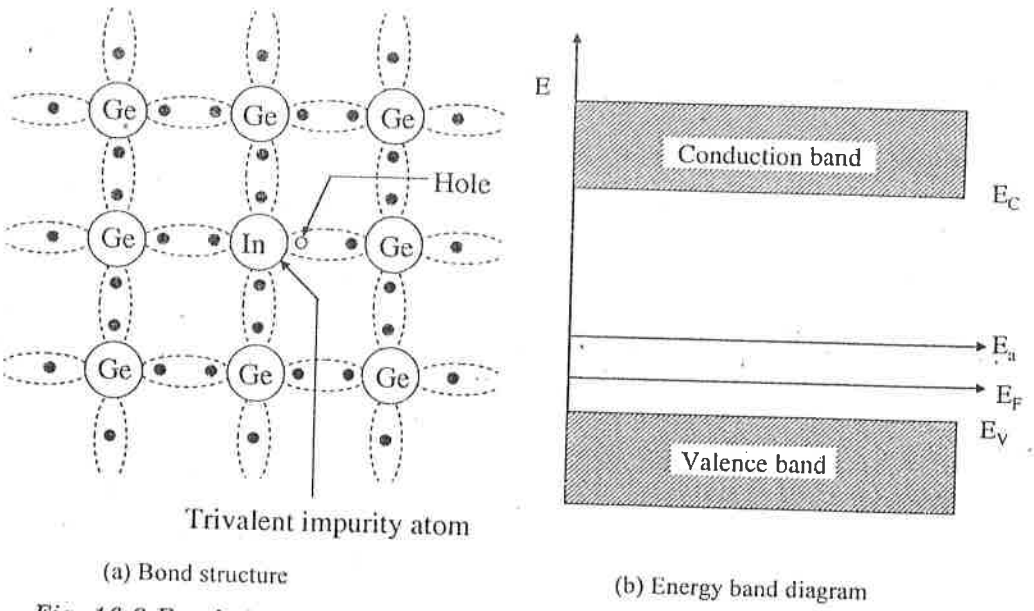
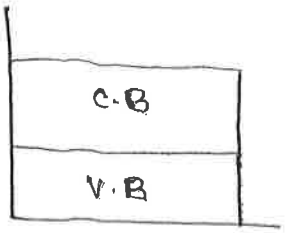
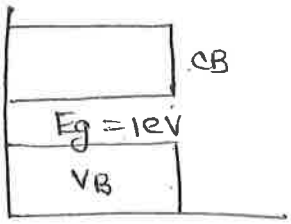
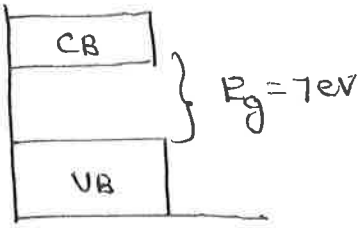


Fig. 16.3 Bond structure and energy band diagram of p-type semiconductor

An impurity that produces holes inside a semiconductor crystal is called acceptor impurity because it accepts electrons from the nearby germanium atoms. The semiconductor containing acceptor type of impurity is called p-type semiconductor, because the charge carriers are positive holes. The energy band diagram for p-type semiconductor is as shown in Fig. 16.3(b). Here E_a represents the energy level corresponding to the accepter impurities. When an intrinsic semiconductor is doped with accepter impurity, the concentration of holes in the valence band will be more than the concentration of electrons in conduction band and the Fermi level shifts towards the valence band. The accepter level is just above the valence band. It should be noted that in p-type semiconductors, holes are majority charge carriers and electrons are the minority charge carriers.

Distinction between Conductors, Semi Conductors and Insulators :-

Conductors	Semi Conductors	Insulators
Energy band diagram is 		
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At room temperature Conductivity is high.	conductivity is in between conductors and Insulators.	conductivity is zero.
Conductivity increases with increase of temperature.	conductivity decreases with increase of Temperature.	
It has positive temperature Coefficient of resistance.	Semiconductors have negative temperature Coefficient of resistance	
Example : Cu	Example : Ge, Si	Ex : Diamond

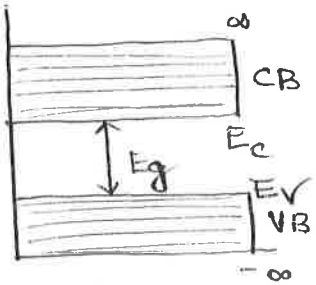
Carrier concentration in Intrinsic Semi conductor :-

In intrinsic Semi conductor the charge carriers are electrons in the conduction band and holes in the valance band. The concentration of Electrons and holes can be obtained from the knowledge of density of available states and as well as Fermi - Dirac distribution function.

Concentration of Electrons in Conduction Band :-

Let us assume the number of states in the Energy range E and E+dE $Z(E)\,dE$ where $Z(E)$ is the density of states. Since each of the state has probability $F(E)$ the Number of Electrons in the range E and E+dE is given by

$$dn = Z(E)\,F(E)\,dE$$



If E_c the Energy of bottom of conduction band

$$n = \int_{E_c}^{\infty} Z(E)\,F(E)\,dE \quad \text{—— (1)}$$

we know that Energy states per unit volume in E and dE+E is

$$Z(E)\,dE = \frac{4\pi}{h^3}(2m)^{3/2}\,E^{1/2}\,dE$$

If m_e^* is the effective mass of an electron

$$Z(E)\,dE = \frac{4\pi}{h^3}\left(2m_e^*\right)^{3/2}\,E^{1/2}\,dE$$

The probability occupation of an electron in the Energy state under thermal Equilibrium is

$$F(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{K_B T}\right)}$$

E_F = Fermi level
K_B = Boltzmann's const
T = Temp in Kelvin

$$F(E) = \left[1 + \exp\left(\frac{E - E_F}{K_B T}\right)\right]^{-1}$$

For all possible temperatures $E - E_F \gg K_B T$

$$\therefore \quad F(E) \approx \exp\left(\frac{E_F - E}{K_B T}\right) \quad \text{---} \quad (3)$$

Substituting 2 and 3 in (1) we get

$$n = \int_{E_c}^{\infty} \frac{4\pi}{h^3} \left(2m_e^*\right)^{3/2} (E - E_c)^{1/2} \exp\left(\frac{E_F - E}{K_B T}\right) dE$$

$$= \frac{4\pi}{h^3} \left(2m_e^*\right)^{3/2} \int_{E_c}^{\infty} (E - E_c)^{1/2} \exp\left(\frac{E_F - E}{K_B T}\right) dE$$

Let us take $E - E_c = x$ $\quad \therefore E = E_c + x$

$$dE = dx$$

$$n = \frac{4\pi}{h^3} \left(2m_e^*\right)^{3/2} \exp\left(\frac{E_F}{K_B T}\right) \int_0^{\infty} x^{1/2} \exp\frac{\left(-E_c \overline{+} x\right)}{K_B T} dx$$

$$n = \frac{4\pi}{h^3} \left(2m_e^*\right)^{3/2} \exp\left(\frac{E_F - E_C}{K_B T}\right) \int_0^{\infty} x^{1/2} \exp\left(\frac{-x}{K_B T}\right) dx$$

Using gamma function we can solve the above equation as

$$\int_0^\infty x^{1/2} \exp\left(\frac{-x}{K_B T}\right) dx = \left(K_B T\right)^{3/2} \frac{\pi^{1/2}}{2}$$

∴ The No of electrons per unit volume of the material is

$$\boxed{n = 2\left(\frac{2\pi m_e^* K_B T}{h^2}\right)^{3/2} \exp\left(\frac{E_F - E_c}{K_B T}\right)} \quad -(4)$$

Concentration of holes in the valance Band :

The No of holes $dp = Z(E)\,(1-F(E))\,dE$

$$1 - F(E) = 1 - \frac{1}{1 + \exp\left[\frac{E-E_F}{K_B T}\right]} = 1 - \left[1 + \exp\left(\frac{E-E_F}{K_B T}\right)\right]^{-1}$$

$$1 - F(E) = \exp\left(\frac{E-E_F}{K_B T}\right) \qquad p = \int Z(E)\,dE\,(1-F(E))\,dE$$

$$Z(E)\,dE = \frac{4\pi}{h^3}\left(2m_h^*\right)^{3/2}\left(E_v - E\right)^{1/2} dE$$

No of holes are

$$p = \int_{-\infty}^{E_v} \frac{4\pi}{h^3}\left(2m_h^*\right)^{3/2}\left(E_v - E\right)^{1/2} \exp\left(\frac{E-E_F}{K_B T}\right) dE$$

$$\boxed{\therefore p = 2\left(\frac{2\pi m_h^* K_B T}{h^2}\right)^{3/2} \exp\left(\frac{E_v - E_F}{K_B T}\right)} \quad -(5)$$

Intrinsic carrier concentration :- According mass action law

$$np = ni^2$$

for intrinsic Semi conductor $n = p$

$$ni^2 = 4\left(\frac{2\pi K_B T}{h^2}\right)^3 \left(m_e^* m_h^*\right)^{3/2} \exp\left(\frac{E_v - E_c}{K_B T}\right)$$

$$ni^2 = 4\left(\frac{2\pi K_B T}{h^2}\right)^3 \left(m_e^* m_h^*\right)^{3/2} \exp\left(\frac{-E_g}{K_B T}\right)$$

$$\therefore ni = 2\left(\frac{2\pi K_B T}{h^2}\right)^{3/2} \left(m_{e_*} m_{h_*}\right)^{3/4} \exp\left(\frac{-E_g}{2K_B T}\right) \quad \text{—(6)}$$

Fermi Level in Intrinsic Semi conductor :- From the Equations 4 and 5

$$2\left(\frac{2\pi m_e^* K_B T}{h^2}\right)^{3/2} \exp\left(\frac{E_F - E_c}{K_B T}\right) = 2\left(\frac{2\pi m_h^* K_B T}{h^2}\right)^{3/2}$$

$$\left(m_e^*\right)^{3/2} \exp\left(\frac{E_F - E_c}{K_B T}\right) = \left(m_h^*\right)^{3/2} \exp\left(\frac{E_v - E_F}{K_B T}\right) \exp\left(\frac{E_v - E_F}{K_B T}\right)$$

$$\text{Exp}\left(\frac{2EF}{K_B T}\right) = \left(\frac{m_h^*}{m_e^*}\right)^{3/2} \exp\left(\frac{E_v + E_c}{K_B T}\right)$$

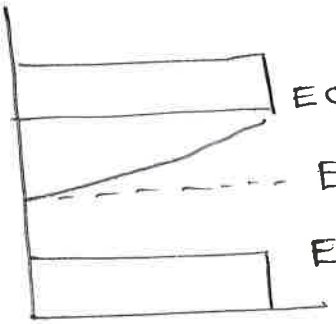
Taking Logenthems on both sides

$$\left(\frac{2E_F}{\quad}\right) = \frac{3}{2} \log\left(\frac{m_h^*}{m_e^*}\right) + \left(\frac{E_v + E_c}{\quad}\right)$$

$$E_F = \frac{3K_BT}{4}\log\left(\frac{m_h^*}{m_e^*}\right) + \left(\frac{E_V + E_C}{2}\right)$$

$\left(\text{If } m_e^* = m_h^*\right)$

$$\therefore \boxed{E_F = \frac{E_V + E_C}{2}}$$



Temperature Vs variation of E_F Level.

Carrier concentration in n-type Semiconductor :- In n type the donar level is just below the conduction Band. Let E_d is the Energy of donar Level and N_d is donar concentration. The concentration of Electronics in CB must be equal to positive ionised donars. We know that

$$n = 2\left(\frac{2\pi m_e^* K_BT}{h^2}\right)^{3/2} \exp\left(\frac{E_F - E_C}{K_BT}\right) \quad \text{---(1)}$$

The No of vaccancies per unit volume in the donar Level is.

$$N_d\left[1 - F(E_d)\right] = N_d\left[1 - \frac{1}{1+\exp\left(\frac{E_d - E_F}{K_BT}\right)}\right]$$

$$= N_d \left[\frac{\exp\left(\frac{E_d - E_F}{K_B T}\right)}{1 + \exp\left(\frac{E_d - E_F}{K_B T}\right)} \right]$$

If $E_F \gg K_B T$

$$N_d \left[1 - F(E_d)\right] = N_d \exp\left(\frac{E_d - E_F}{K_B T}\right)$$

No of Electrons = No of ionised Donars

$$2\left(\frac{2\pi m_e^* K_B T}{h^2}\right)^{3/2} \exp\left(\frac{E_F - E_c}{K_B T}\right) = N_d \exp\left(\frac{E_d - E_F}{K_B T}\right)$$

Taking Logenthems

$$\left(\frac{E_F - E_c}{K_B T}\right) - \left(\frac{E_d - E_F}{K_B T}\right) = \log N_d - \log_2 \left(\frac{2\pi m_e^* K_B T}{h^2}\right)^{3/2}$$

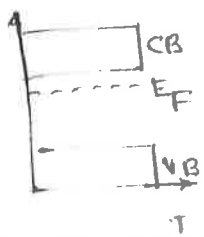
$$2E_F - (E_d + E_c) = K_B T \log \frac{N_d}{2\left(\frac{2\pi m_e^* K_B T}{h^2}\right)^{3/2}}$$

$$E_F = \left(\frac{E_d + E_c}{2}\right) + \frac{K_B T}{2} \log \left(\frac{N_d}{2\left(\frac{2\pi m_e^* K_B T}{h^2}\right)^{3/2}} \right)$$

—(2)

Substituting (2) in (1) we get

$$n = (2N_d)^{1/2} \left(\frac{2\pi m_e^* K_B T}{h^2}\right)^{3/4} \exp\left(\frac{E_d - E_c}{2K_B T}\right)$$



Carrier Concentration in p type Semi conductor :-

In p type semi conductor the acceptor level is just above the valance band as shown. Let E_a represent the Energy of acceptor level and N_a is the acceptor concentration. The density of holes in the valance band is given by

$$p = 2\left(\frac{2\pi m_h^* K_B T}{h^2}\right)^{3/2} \exp\left(\frac{E_v - E_F}{K_B T}\right) \quad \text{---} \ (1)$$

The density of ionized acceptors is given by

$$N_a F(N_a) = \frac{N_a}{1 + \exp\left(\frac{E_a - E_F}{K_B T}\right)}$$

If $E_a - E_F \gg K_B T$

$$N_a F(E_a) = N_a \cdot \exp\left(\frac{E_F - E_a}{K_B T}\right)$$

The density of holes = the density of negative acceptors

$$2\left(\frac{2\pi m_h^* K_B T}{h^2}\right)^{3/2} \exp\left(\frac{E_v - E_F}{K_B T}\right) = N_a \exp\left(\frac{E_F - E_a}{K_B T}\right)$$

$$\exp\left(\frac{E_v + E_a - 2E_F}{K_B T}\right) = \frac{N_a}{2\left(\frac{2\pi m_h^* K_B T}{h^2}\right)^{3/2}}$$

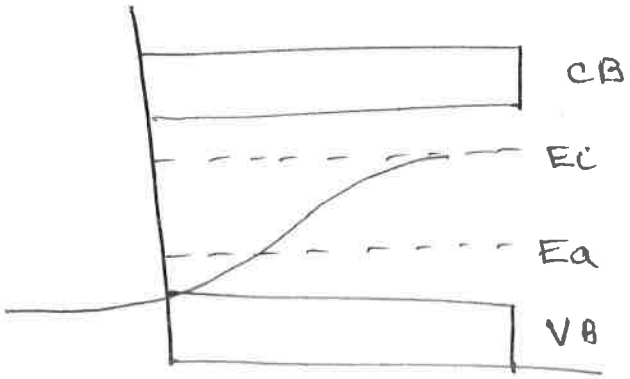
Taking logenthems and re-arranging the terms

$$p = (2N_a)^{1/2} \left(\frac{2\pi m h^* K_B T}{h^2} \right)^{3/4} \exp\left(\frac{E_V - E_a}{2K_B T} \right)$$

$$E_F = \left(\frac{E_V + E_a}{2} \right) - \frac{K_B T}{2} \log \frac{N_a}{2\left(\frac{2\pi m h^* K_B T}{h^2} \right)^{3/2}}$$

at $T = 0^\circ K$

$$E_F = \left(\frac{E_V + E_a}{2} \right) \checkmark$$



Variation of Fermi Level with Temperature

Drift and Diffusion currents :-

Drift current

1. The current due to holes and electrons in a semi conductor in the prexence of applied electric field is called as drift current. The average velocity attained by caniers is called as drift velocity.

2. Drift velocity V_d is proportional to applied electric field $\bar{E}$.

$$V_d \propto E$$

$$V_d = \mu E$$

Here μ = Hobility of Electrons

3. The current density $J = nev_d$

$$\boxed{J = ne\mu E}$$

4. Drift current due to electrons

$$J_n(\text{drift}) = ne\mu_n E$$

5. Drift current due to holes

$$J_p(\text{drift}) = pe\mu_p E$$

6. Total current (drift) : $J = \sigma E$

$$J = (n\mu_n + p\mu_p)eE$$

Diffusion current

1. It is the current due to diffusion of caniers from high concentration to low concentration i.e it flows due to concentration gradient.

2. The diffusion current is proportional to the concentration gradient.

$$J_n \propto \frac{dn}{dx}$$

$$J_n(\text{diffusion}) = eD_n\frac{dn}{dx}$$

$$J_p(\text{diffusion}) = -eD_p\frac{dp}{dx}$$

Here D_p, D_n are diffusion consts for holes and electrons.

$$J_{\text{diffusion}} = J_n + J_p$$

$$= -eD_p\frac{dp}{dx} + eD_n\frac{dn}{dx}$$

Note that hole and electron diffusion currents are in opposite directions in a semiconductor.

Total current In a Semiconductor :-

$$J = J_{drift} + J_{diffusion}$$

$$J = eE\left(n\mu_n + p\mu_p\right) - e D_p \frac{dp}{dx} + e D_n \frac{dn}{dx}$$

$$J = e\left[\left[n\mu_n E + D_n \frac{dn}{dx}\right] + \left[\left(p\mu_p E - D_p \frac{dp}{dx}\right)\right]\right]$$

Einestain's Equation :- The mobility of carriers expresses the ability of carriers to drift and diffusion const D expresses the ability of carriers to diffuse. Einestain relates the concepts of mobility and diffusion const D.

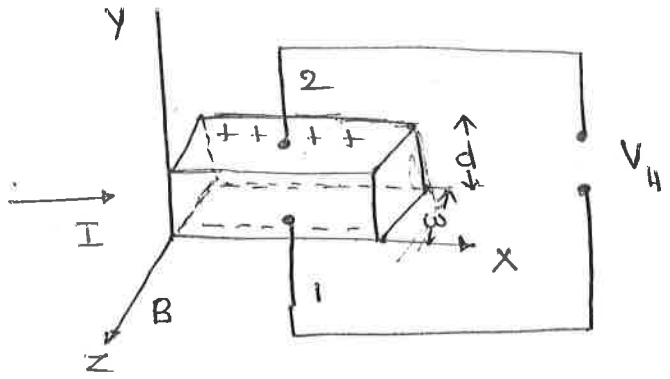
$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{K_B T}{e}$$

Here D_n, D_p are diffusion constants for holes and electrons

μ_p, μ_n are Mobilities for holes and electrons.

According to Einestains Equation the ratio of diffusion const and Mobility is directly proportional to Absolute Temperature. It also tells that D, μ increases with Temperature.

Hall effect :-



If a specimen carrying current I is placed in a Transverse magnetic field, an Electric field will be induced in the direction perpendicular to Both I and B. This phenomenon is called as Hall effect. If I is in +ve X direction and B is in +z direction a force will be exerted in −Y direction. The current I may be due to holes or electrons flow in a bar. Irrespective of the carriers they will be forced to side 1. If the bar is n type, Electrons will be accumulated on side 1, this surface becomes -ve charged with respect to 2. Hence Hall voltage will be produced between 1 and 2.

If V_H is +ve the semi conductor is n type.

If V_H is -ve the semi conductor is p type.

Mathematical Analysis :- Under equilibrium state the Hall effect will balance the Magnetic force (i.e balancing of forces)

$$\therefore \quad eE = Bev \qquad (v \text{ is the drift velocity})$$

$$\text{we Know} \quad E = \frac{V_H}{d}$$

$$\text{The current density} \quad J = pv = \frac{I}{wd}$$

If V_H, B, I, w are measured p can be calculated.

Hall coefficient $R_H = \frac{1}{p}$

$$\therefore \boxed{R_H = \frac{V_H w}{BI}}$$

and Mobility $\mu = \sigma R_H \quad (\because \sigma = p\mu)$

$$R_H = \frac{E_H}{JB} = -\frac{1}{ne} \qquad R_H = \frac{E_H}{JB} = \frac{1}{pe}$$

Applications :-

1. The sign of the charge carriers can be determined i.e it tells whether the specimen is p type or N type
2. It is used to calculate current density
3. It determines mobility of the carriers.
4. It determines whether the given material is insulator, conductor or Semi conductor
5. It measures the Magnetic field also

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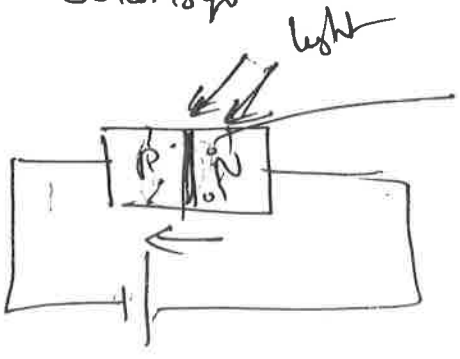
photo conductors : Solar cell

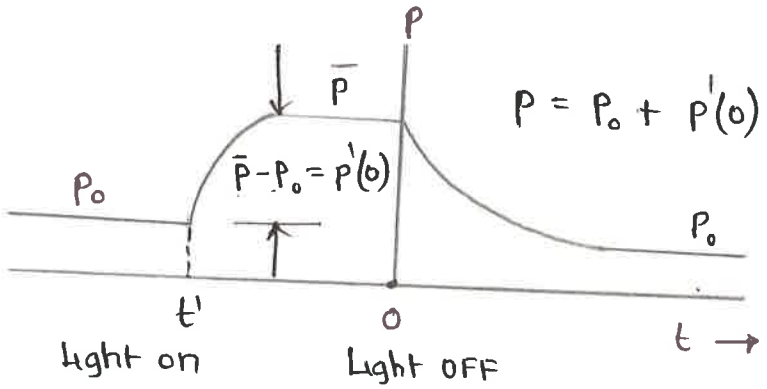


minority carri
min

$\lambda_c = \frac{hc}{E_g}$

UNIT - II

Generation and Recombination of charges :- Consider a bar of n type Silicon containing thermal equilibrium concentrations P_o and n_o as shown below.



Assume that at $t = t'$ the light is turned on and that additional holes and electrons are generated and the new values are $\bar{P}$ and $\bar{n}$. The injected concentrations are $\bar{P} - P_o$ for holes and $\bar{n} - n_o$ for electrons.

At $t = b$, the radiation is removed and the excess concentration exponentially decreases and reaches to the final value P_o.

According to law of conservation of charge

$$\frac{dp}{dt} = g - P/\tau_p$$

Here g = increase in holes due to thermal

$\frac{P}{\tau_p}$ = decrease in holes due to recombination

Under steady state $\frac{dp}{dt} = 0$

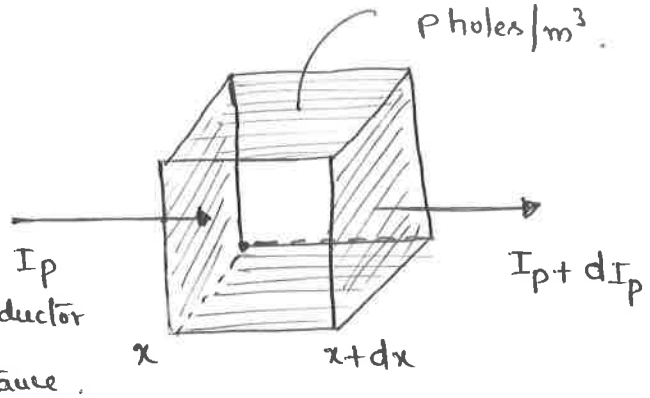
$$\therefore g = \frac{P_o}{\tau_p} \qquad \therefore \frac{dp}{dt} = \frac{P_o - P}{\tau_p} = \frac{-P'}{\tau_p}$$

Finally we have

$$\boxed{P = P_o + P'(0) \cdot e^{-t/\tau_p}}$$

Recombination : It is the process where the electron moves from

Continuity Equation :-



The carrier concentration in a semiconductor is a function of both time and distance.

We can derive the differential equation which governs the relationship. consider the Element of area A and length dx and the average hole concentration is P.

Let the current at the x is I_p and at x+dx is $I_p + dI_p$

i.e there is dI_p more coloumbs/second leaving the volume than entering. Since the magnitude of the charge is q, then $\frac{dI_p}{q}$ equals the decreax in no of holes per second within the volume Adx.

$$\therefore \frac{1}{qA}\frac{dI_p}{dx} = \frac{1}{q}\cdot\frac{dJ_p}{dx}$$

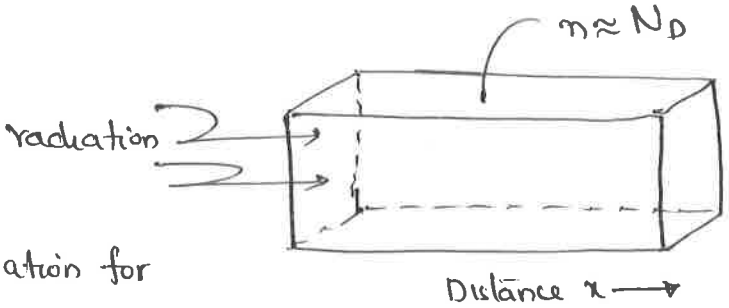
According to generation and recombination of charges

$$\frac{\partial P}{\partial t} = \frac{P_0 - P}{\tau_p} - \frac{1}{q}\frac{dJ_p}{dx}$$

The above equation is Law of conservation of charge (or) continuity equation for charge.

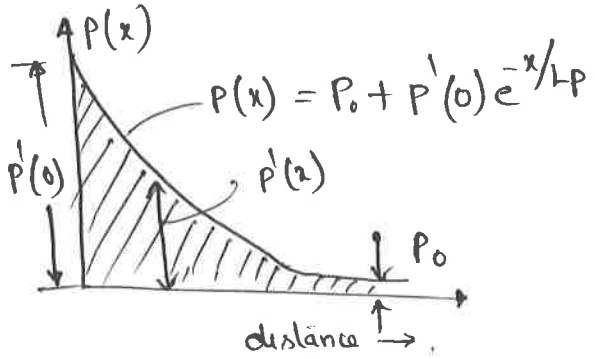
Injected Minority - carrier charge :-

Let us consider a bar of N type semiconductor in which minority concentration is much smaller than majority concentration and the drift current is also negligible.



The differential equation for holes is

$$\frac{d^2p}{dx^2} = \frac{P - P_0}{D_p \tau_p}$$



Defining the diffusion length of the carriers $L_p \equiv (D_p \tau_p)^{1/2}$

Then the differential equation

$$\frac{d^2p'}{dx^2} = \frac{p'}{L_p^2}$$

writing the solution for 2nd order differential equation we can write

$$\boxed{p'(x) = p'(0)\, e^{-x/L_P} = P(x) - P_0.}$$

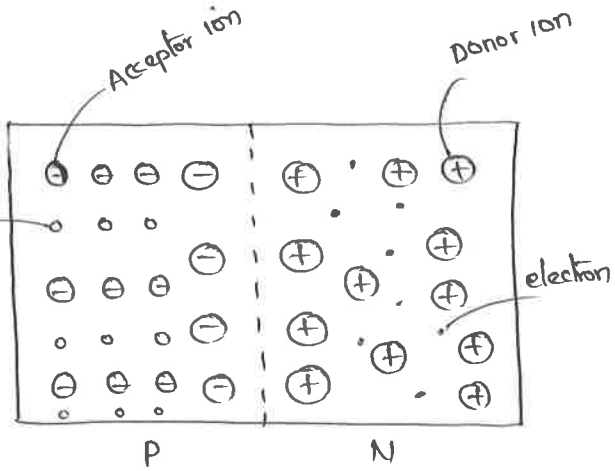
Potential variation within a Giraded Semiconductor :—
(Law of Junction, Barrier potential)

Consider a Semi conductor where the hole concentration p is a function of 'x'. i.e the doping is non uniform or graded. Assuming steady state situation and zero excitation we can conclude that hole current must be zero. As p is constant there may be non zero diffusion current. Hence to make the total current zero, there must be drift current in opposite direction. However, a conduction current requires an electric field. Electric field will be generated as a result of non-

UNIT - III Junction Diode characteristics

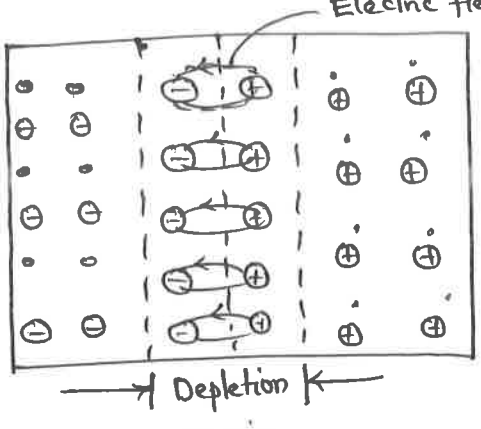
✓ If donor impurities are introduced on one side and acceptors into the other side of a single crystal of Semi conductor a p-n Junction is formed. The most important characteristic of a P-N Junction is its ability to conduct in one direction only.

Open circuited P-N Junction : The figure shows a P-N Junction just immediately it is formed. Its left half is P type and Right half is N type. Holes and electrons are the mobile charges and the ions are immobile.



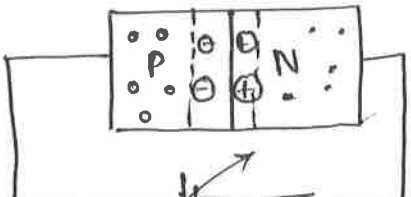
Note that no external voltage is connected to the given PN Junction. when P-n Junction is formed the following processes are initiated.

1) Holes from P ~~type~~ region diffuse into N region they combines with free electrons in N-region
2) Diffusion of electrons from N type to p region and combine with the holes in P- region.
3) The diffusion of holes and electrons occurs for a very short time. After few recombinations of holes and electrons in the immediate neighbourhood of the Junction a restraining force is set up automatically. This force is called barrier.
4) Some of the holes in the P region and some of the electrons in the n region diffuse toward each other and recombine. Each recombination eliminates a hole and a free electron. Thus the depletion region will be formed as shown in the figure. That is, there is depletion of mobile charges in this region. It is called as space charge region. The potential across this barrier is called as barrier potential. For Germanium it is 0.3V and for silicon it is 0.6V.



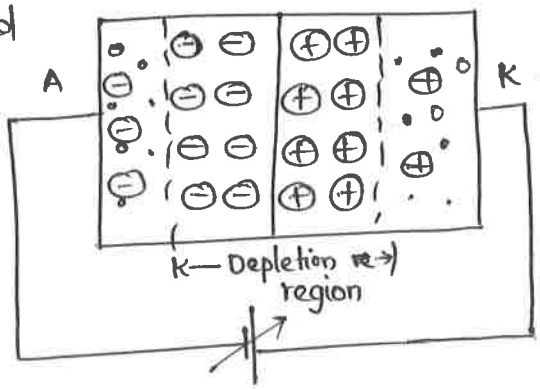
PN Junction with Forward Bias :-

The diode is said to be in forward Bias whenever the +ve terminal of the Battery is connected to Anode and -ve terminal of the



when the PN Junction is forward Biased the holes are repelled from +ve terminal of the battery and are moved towards the Junction. Similary the electrons move towards the Junction repelled from -ve terminal of Battery. Heuce the width of the depletion region decreases and more carriers cross the Junction. Heuce maximum current flows through the diode in forward Bias.

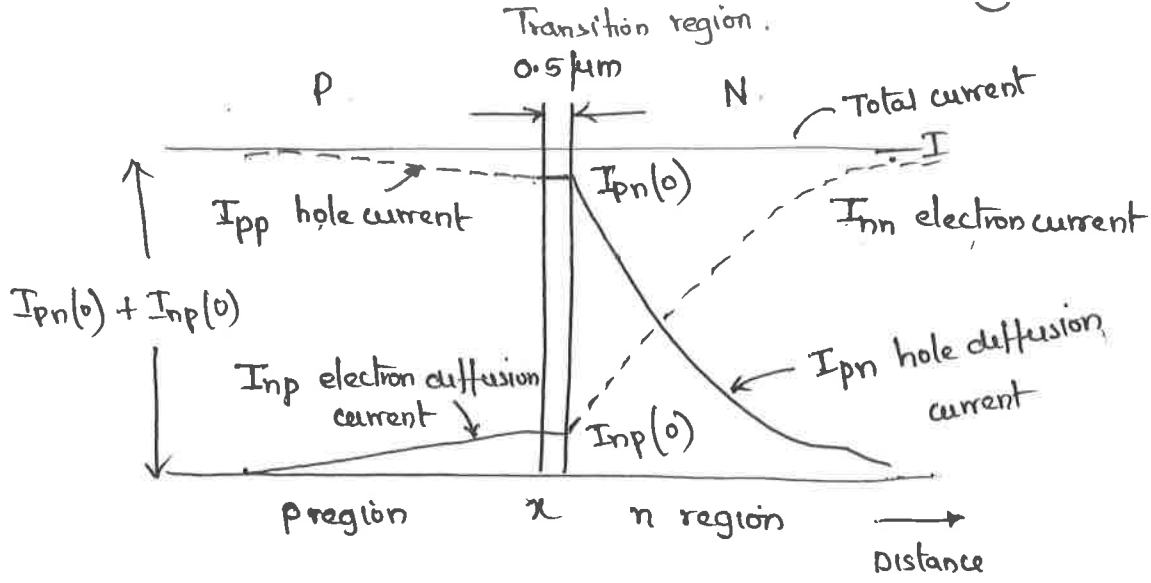
PN Junction with Reverse Bias :- If the +ve terminal is connected to cathode and -ve terminal to Anode the diode is saidtobe in reverse Bias. The holes are attracted towards negative terminal and electrons towards positive terminal. Thus the majority carriers are drawn from the Junction. This action widens the depletion region and increases the barrier potential. The increased



barrier potential makes it more difficult for the majority carriers to diffuse across the Junction. But the reverse bias is helpful for the minority carriers to cross the Junction. Infact as soon as the minority carriers are generated they will swept across the Junction ~~as~~ because of the barrier potential. The rate of generation of minority carriers depends upon temperature. The current due to minority carriers is called as reverse saturation current (I_0). It is of the order of nano ampers in silicon diode and microampers in Germanium diodes.

The current components in a PN Diode :-

when forward Bias is applied holes are injected into n side and electrons are into p side. Assuming the p side is heavily doped compared to n type the current components are drawn and shown in the figure. Solid line indicates ~~majority~~ minority currents and dotted line indicates majority currents.



Here The Majority current $I_{nn}(x) = I - I_{pn}(x)$

I_{pp} is the hole drift current which decreases towards the junction as the holes recombine with the electrons which are injected into p side from n region. Then the current I_{pp} becomes hole diffusion current $I_{pn}(x)$ in the n region. Similarly I_{nn} is the electron drift current and it becomes $I_{np}(x)$ (electron diffusion current) in p region.

Diode current Equation :- It is well known that the minority hole diffusion current in 'n' region is given by $I_p = A J_p$ — (1)

From the definition of diffusion current $J_p = -q D_p \frac{dp}{dx}$ — (2)

Substituting 1 in 2 we have

$$I_p = -Aq D_p \frac{dp}{dx} \quad \text{but} \quad \frac{dp}{dx} = p(x) - p_0 = p'(0)\, e^{-x/L_p}$$

$$\therefore \quad I_p = -Aq D_p \frac{d}{dx}\left(p'(0)\, e^{-x/L_p}\right)$$

$$I_p = -Aq D_p\, p'(0)\, e^{-x/L_p} \cdot -1/L_p$$

$$I_p = \frac{Aq D_p}{L_p}\left[p(0) - p_0\right] e^{-x/L_p}$$

at $x = 0$ using the appropriate notation we have

✓ Law of Junction :- It is known that Forward Bias lowers the barrier height and allows more carriers to cross the Junction. Hence $P_n(0)$ is a function of V

$$P_n(0) = P_{no}\, e^{V/V_T} \quad \text{—— (4)}$$

The above relation-ship gives the hole concentration at the edge of 'n' region at $x=0$ in terms of thermal equilibrium minority carrier concentration. and the applied potential 'V' is called the Law of Junction.

Substituting 4 in 3 we have

$$I_{pn}(x) = \frac{Aq D_p}{L_p}\left(P_{no}\, e^{V/V_T} - P_{no}\right) e^{-x/L_p}$$

at $x=0$ we have

$$I_{pn}(0) = \frac{Aq D_p}{L_p}\left(e^{V/V_T} - 1\right) P_{no} \quad \text{—— (5)}$$

similary the expression for electron diffusion current

$$I_{np}(0) = \frac{Aq D_n}{L_n}\left(e^{V/V_T} - 1\right) n_{po} \quad \text{— (6)}$$

The total Diode current $I = I_{pn}(0) + I_{np}(0)$

$$\therefore I = Aq\left(e^{V/V_T} - 1\right)\left(\frac{D_p}{L_p} P_{no} + \frac{D_n}{L_n} \cdot n_{po}\right)$$

From the charge Densities we have

$$P_{no} = \frac{n_i^2}{N_D} \qquad n_{po} = \frac{n_i^2}{N_A}$$

$$\therefore I = Aq n_i^2 \left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right)\left(e^{V/V_T} - 1\right)$$

✓ $$\boxed{\therefore \quad I = I_0\left(e^{V/\eta V_T} - 1\right)}$$

$\eta = 1$ Ge
$\eta = 2$ Si

$I_0 = Aq\left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right) n_i^2$

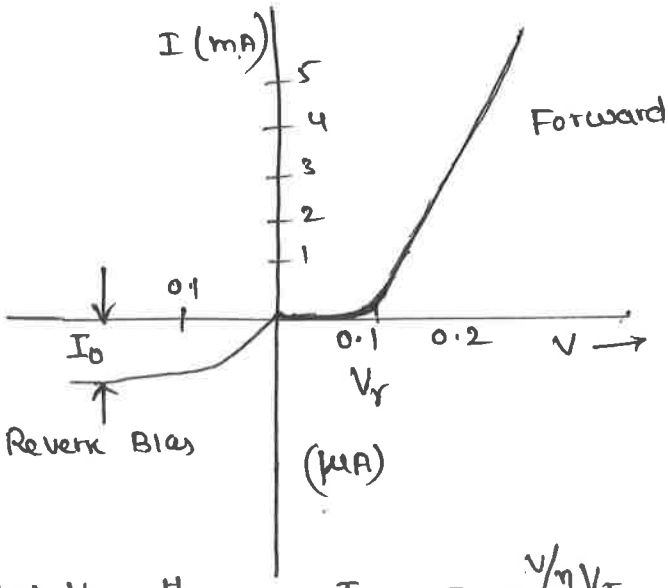
The volt-Ampere characteristics :- For a pn junction diode we have

$$I = I_0 \left(e^{V/\eta V_T} - 1 \right)$$

Here $V_T = \frac{T}{11,600}$ and at room temp $(T = 300^\circ K)$ $V_T = 26mV$

η depends on material. and V is +ve for Forward Bias.

By plotting the graph between V and I we have



For Forward Bias $V \gg V_T$ then $I = I_0 e^{V/\eta V_T}$. $\left(\because e^{V/\eta V_T} \gg 1 \right)$

Then the current increases exponentially.

For Reverse Bias $|V| \gg V_T$ then $\boxed{I = -I_0}$

The Voltage at which the current increases suddenly is called as cutin, offset, break point or thershold voltage.

Temperature dependence on VI characteristics :- From the relation between V and I of a diode i.e $I = I_0 \left(e^{V/\eta V_T} - 1 \right)$ it is evident that current I depends on V_T and reverse saturation current (I_0) which are depending on Temperature.

It can be shown that I_0 changes with T at 8 percent/°c for Si and 11 percent/°c for Ge.

From experimental data we observe that I_o increases approximately 7 percent/°c for both silicon and Germanium.

Since $(1.07)^{10} \approx 2.0$

Therefore the reverse saturation current approximately doubles for every 10°c rise in temperature.

If $I_o = I_{o1}$ at $T = T_1$ then at a temperature T, I_o is given by

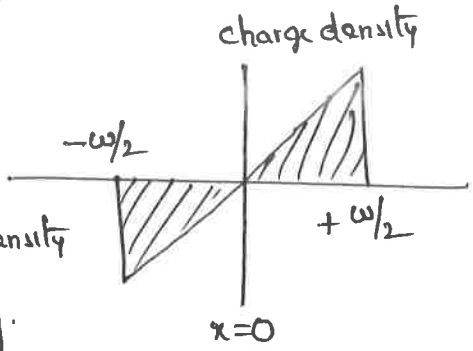
$$\boxed{I_o(T) = I_{o1} \times 2^{(T-T_1)/10}}$$

If the temperature is increased at a fixed voltage

$$\boxed{\frac{dv}{dT} \approx -2.5 \text{ mv}/^\circ\text{c}}$$

Step Graded Junction :- It is a junction in which there is an abrupt change from acceptor ions on one side to donor ions on the otherside. Such a junction is formed by placing Indium against n type germanium and heating the combination to high temperature for a short time. Such a step graded junction is called an alloy or fusion junction. Ex : Emitter junction in a Transistor.

Linearly Graded Junction :-



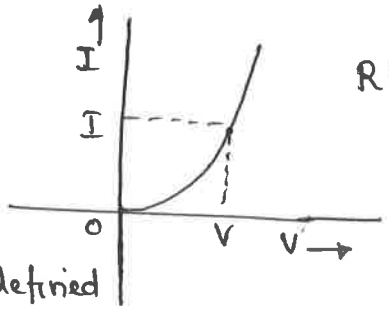
In this type of junction the charge density varies gradually i.e almost linearly.

Ex : collector junction in Transistor.

This type of junction is obtained by drawing a single crystal from a melt of germanium whose type is changed during the drawing process

Diode Resistance : There are two types of Resistances.

i) **Static Resistance** :- The static resistance R of a diode is defined as the ratio of voltage to current at any point on the Volt ampere characteristic. It varies widely with V and I and not a useful parameter. It is also called as DC resistance.



ii) AC or dynamic resistance :- It is defined as the reciprocal of the slope of the Volt-ampere characteristic. It is also called as incremental resistance.

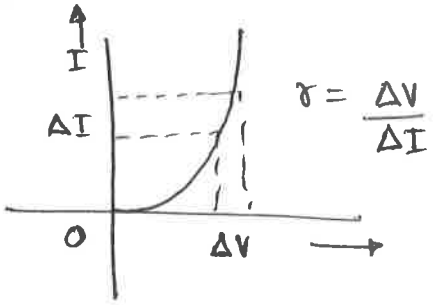
$$\therefore g = \frac{dI}{dV} \qquad I = I_0\left(e^{V/\eta V_T} - 1\right)$$

$$g = \frac{d}{dV}\left(I_0\left(e^{V/\eta V_T} - 1\right)\right)$$

$$g = \frac{I_0 \cdot e^{V/\eta V_T}}{\eta V_T} = \frac{I + I_0}{\eta V_T}$$

As $I_0 << I$ then

$$g = \frac{I}{\eta V_T} \quad \therefore \quad \boxed{r = \frac{\eta V_T}{I}}$$



The dynamic resistance is inversely proportional to I.

Diode Capacitance :- There are two types of capacitances

i) **Transision capacitance C_T :-** under reverse Bias condition the majority carriers move away from the Junction, thereby uncovering more immobile charges. Hence the depletion region width increases with reverse voltage. This increase in the uncovered charge with applied voltage

Incremental capacitance $C_T = \left|\frac{dQ}{dV}\right|$

$\therefore \quad dQ = C_T \cdot dV$

$$\frac{dQ}{dt} = C_T \cdot \frac{dV}{dt}$$

$$\boxed{i = C_T \frac{dV}{dt}}$$

The quantity C_T is called as space charge, barrier, depletion region capacitance.

For a reverse biased diode we can prove that

$$\boxed{C_T = \frac{\epsilon A}{w}}$$

Here w = width of the depletion region.

Diffusion Capacitance :- This capacitance is predominant in forward bias. The origin of this larger capacitance lies in the injected charge stored near the junction outside the transition region. It is defined as the rate of change of injected charge with voltage called the diffusion or storage capacitance C_D.

Derivation :- we know that $C_D = \frac{dQ}{dV} = \tau \frac{dI}{dV} = \tau g = \frac{\tau}{r}$

$$\therefore \quad C_D = \frac{\tau}{\eta V_T / I} = \frac{\tau I}{\eta V_T}.$$

$$\therefore \quad \boxed{C_D = \frac{\tau I}{\eta V_T}}$$

i.e diffusion capacitance is proportional to I.

Total diffusion capacitance $C = C_{Dp} + C_{Dn}$

Here C_{Dp} = diffusion capacitance due to holes

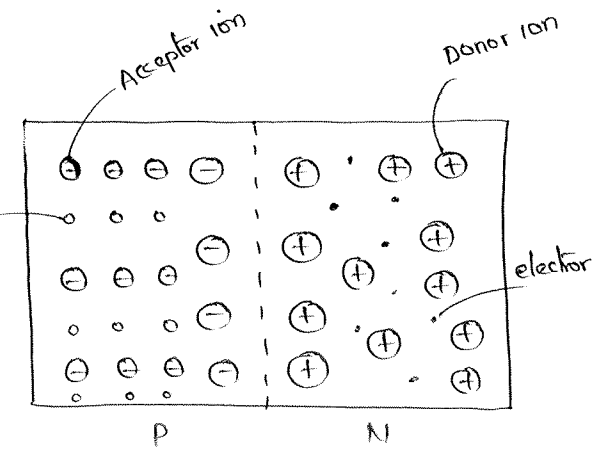
C_{Dn} = diffusion capacitance due to electrons.

UNIT - III Junction Diode characteristics

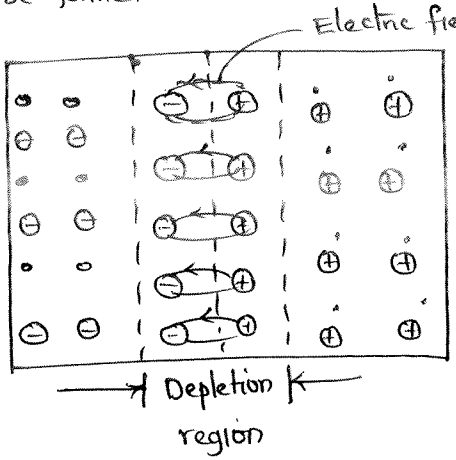
✓ If donor impurities are introduced on one side and acceptors into the other side of a single crystal of Semi conductor a P-n Junction is formed. The most important characteristic of a P-N junction is its ability to conduct in one direction only.

Open circuited P-N Junction : The figure shows a P-N Junction just immediately it is formed. Its left half is P type and Right half is N type. Holes and electrons are the mobile charges and the ions are immobile.

Note that no external voltage is connected to the given PN Junction. when P-n junction is formed the following processes are initiated.

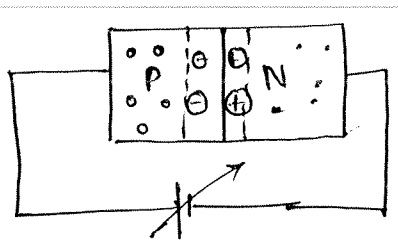


1) Holes from P type region diffuse into N region they combines with free electrons in N-region
2) Diffusion of electrons from N type to p region and combine with the holes in P- region.
3) The diffusion of holes and electrons occurs for a very short time. After few recombinations of holes and electrons in the immediate neighbourhood of the Junction a restraining force is setup automatically. This force is called barrier.
4) Some of the holes in the P region and some of the electrons in the n region diffuse toward each other and recombine. Each recombination eliminates a hole and a free electron. Thus the depletion region will be formed as shown in the figure. That is, there is depletion of mobile charges in this region. It is called as space charge region. The potential across this barrier is called as barrier potential. For Germanium it is 0.3V and for silicon it is 0.6V.



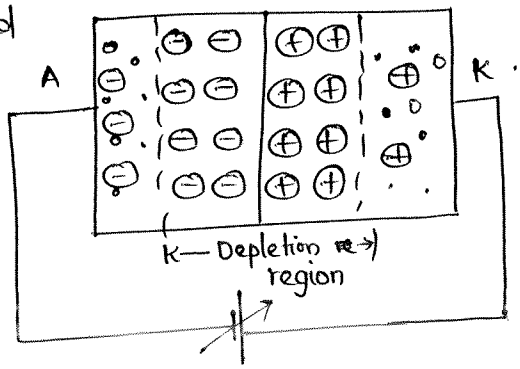
PN Junction with Forward Bias :-

The diode is said to be in forward Bias whenever the +ve terminal of the Battery is connected to Anode and -ve terminal of the Battery is connected to cathode.



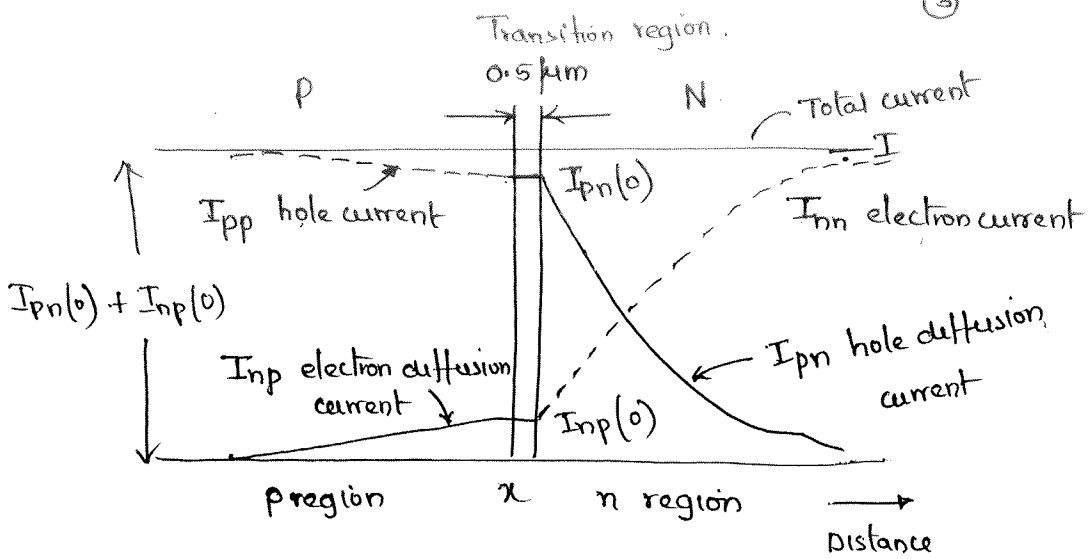
when the PN Junction is forward Biased the holes are repelled from +ve terminal of the battery and are moved towards the Junction. Similary the electrons move towards the Junction repelled from -ve terminal of Battery. Hence the width of the depletion region decreases and more carriers cross the Junction. Hence maximum current flows through the diode in forward Bias.

PN Junction with Reverse Bias :- If the +ve terminal is connected to cathode and -ve terminal to Anode the diode is said to be in reverse Bias. The holes are attracted towards negative terminal and electrons towards positive terminal. Thus the majority carriers are drawn from the Junction. This action widens the depletion region and increases the barrier potential. The increased barrier potential makes it more difficult for the majority carriers to diffuse across the Junction. But the reverse bias is helpful for the minority carriers to cross the Junction. Infact as soon as the minority carriers are generated they will swept across the Junction because of the barrier potential. The rate of generation of minority carriers depends upon temperature. The current due to minority carriers is called as reverse saturation current (I_0). It is of the order of nano ampers in silicon diode and microampers in Germanium diodes.



The current components in a PN Diode :-

when forward Bias is applied holes are injected into n side and electrons are into p side. Assuming the p side is heavily doped compared to n type the current components are drawn and shown in the figure. Solid line indicates minority currents and dotted line indicates majority currents.



Here The Majority current $I_{nn}(x) = I - I_{pn}(x)$

I_{pp} is the hole drift current which decreases towards the junction as the holes recombine with the electrons which are injected into p side from n region. Then the current I_{pp} becomes hole diffusion current $I_{pn}(x)$ in the n region. Similarly I_{nn} is the ~~h~~ electron drift current and it becomes $I_{np}(x)$ (electron diffusion current) in p region.

Diode current Equation :- It is well known that the minority hole diffusion current in 'n' region is given by $I_p = A J_p$ —(1)

From the definition of diffusion current $J_p = -q D_p \frac{dp}{dx}$ —(2)

Substituting 1 in 2 we have

$$I_p = -Aq D_p \frac{dp}{dx} \quad \text{but} \quad \frac{dp}{dx} = p(x) - p_0 = p'(0)\, e^{-x/L_p}$$

$$\therefore \quad I_p = -Aq D_p \frac{d}{dx}\left(p'(0)\, e^{-x/L_p}\right)$$

$$I_p = -Aq D_p\, p'(0)\, e^{-x/L_p} \cdot -1/L_p$$

$$I_p = \frac{Aq D_p}{L_p}\left[p(0) - p_0\right] e^{-x/L_p}$$

at $x = 0$ using the appropriate notation we have.

$$I_{pn}(0) = \frac{Aq D_p}{L_p}\left(p_n(0) - p_{n0}\right) e^{-x/L_p} \quad \text{—— (3)}$$

✓ Law of Junction :- It is known that Forward Bias lowers the barrier height and allows more carriers to cross the Junction. Hence $P_n(0)$ is a function of V

$$P_n(0) = P_{no}\, e^{V/V_T} \quad \text{—— (4)}$$

The above relation-ship gives the hole concentration at the edge of 'n' region at $x=0$ in terms of thermal equilibrium minority carrier concentration. and the applied potential 'V' is called the Law of Junction.

Substituting 4 in 3 we have

$$I_{pn}(x) = \frac{Aq D_p}{L_p}\left(P_{no}\, e^{V/V_T} - P_{no}\right) e^{-x/L_p}$$

at $x=0$ we have

$$I_{pn}(0) = \frac{Aq D_p}{L_p}\left(e^{V/V_T} - 1\right) P_{no} \quad \text{—— (5)}$$

similary the expression for electron diffusion current

$$I_{np}(0) = \frac{Aq D_n}{L_n}\left(e^{V/V_T} - 1\right) n_{po} \quad \text{— (6)}$$

The total Diode current $I = I_{pn}(0) + I_{np}(0)$

$$\therefore I = Aq\left(e^{V/V_T} - 1\right)\left(\frac{D_p}{L_p} P_{no} + \frac{D_n}{L_n} \cdot n_{po}\right)$$

From the charge Densities we have

$$P_{no} = \frac{n_i^2}{N_D} \qquad n_{po} = \frac{n_i^2}{N_A}$$

$$\therefore I = Aq n_i^2 \left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right)\left(e^{V/V_T} - 1\right)$$

✓ $$\boxed{\therefore \quad I = I_0\left(e^{V/\eta V_T} - 1\right)}$$

$\eta = 1$ Ge
$\eta = 2$ Si

Here I_0 = reverse saturation current = $Aq\left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right) n_i^2$

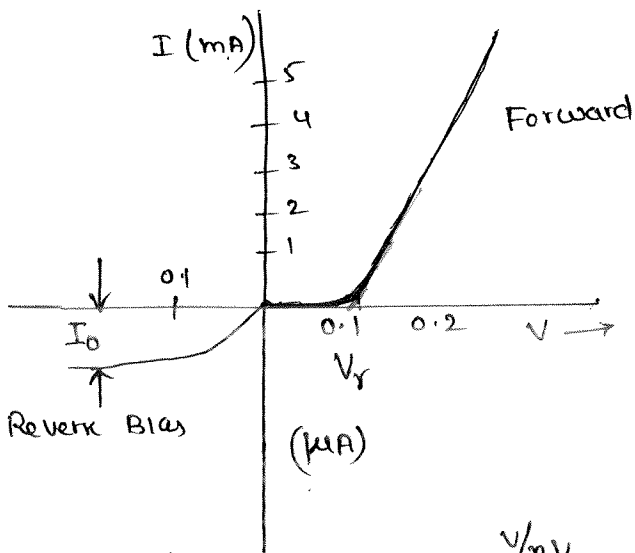
The volt - Ampere characteristics :- For a pn junction diode we have

$$I = I_0 \left(e^{V/\eta V_T} - 1 \right)$$

Here $V_T = \frac{T}{11,600}$ and at room temp ($T = 300^\circ K$) $V_T = 26mV$

η depends on material. and V is +ve for Forward Bias.

By plotting the graph between V and I we have



For Forward Bias $V \gg V_T$ then $I = I_0 e^{V/\eta V_T}$. $\left(\because e^{V/\eta V_T} \gg 1 \right)$

Then the current increases exponentially.

For Reverse Bias $|V| \gg V_T$ then $\boxed{I = -I_0}$

The voltage at which the current increases suddenly is called as cut in, offset, break point or threshold voltage.

Temperature dependence on VI characteristics :- From the relation between V and I of a diode i.e $I = I_0 \left(e^{V/\eta V_T} - 1 \right)$ it is evident that current I depends on V_T and reverse saturation current (I_0) which are depending on Temperature.

It can be shown that I_0 changes with T at 8 percent/°c for Si and 11 percent/°c for Ge.

From experimental data we observe that I_o increases approximately 7 percent/°c for both silicon and Germanium.

Since $(1.07)^{10} \approx 2.0$

Therefore the reverse saturation current approximately doubles for every 10°c rise in temperature.

If $I_o = I_{o1}$ at $T = T_1$ then at a temperature T, I_o is given by

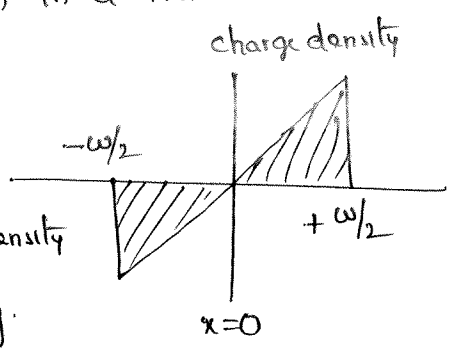
$$\boxed{I_o(T) = I_{o1} \times 2^{(T-T_1)/10}}$$

If the temperature is increased at a fixed voltage

$$\boxed{\frac{dV}{dT} \approx -2.5 \text{ mv}/^{\circ}\text{c}}$$

Step Graded Junction :- It is a junction in which there is an abrupt change from acceptor ions on one side to donor ions on the otherside. Such a junction is formed by placing indium against n type germanium and heating the combination to high temperature for a short time. Such a step graded junction is called an alloy or fusion junction. Ex : Emitter junction in a Transistor.

Linearly Graded Junction :-



In this type of junction the charge density varies gradually i.e almost linearly.

Ex : collector junction in Transistor.

This type of junction is obtained by drawing a single crystal from a melt of germanium whose type is changed during the drawing process by adding first p type and n type impurities.

Diode Resistance : There are two types of Resistances.

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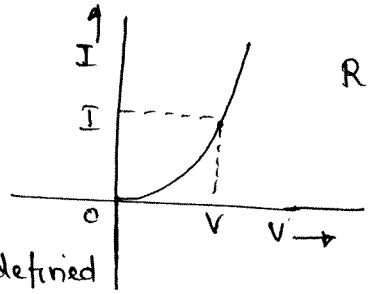
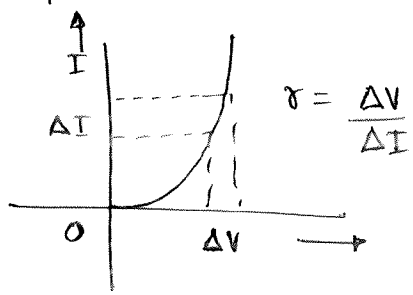


ii) **Ac or dynamic resistance :-** It is defined as the reciprocal of the slope of the Volt-ampere characteristic. It is also called as incremental resistance.



$$\therefore g = \frac{dI}{dV} \qquad I = I_0\left(e^{V/\eta V_T} - 1\right)$$

$$g = \frac{d}{dV}\left(I_0\left(e^{V/\eta V_T} - 1\right)\right)$$

$$g = \frac{I_0 \cdot e^{V/\eta V_T}}{\eta V_T} = \frac{I + I_0}{\eta V_T}$$ As $I_0 << I$ then

$$g = \frac{I}{\eta V_T} \quad \therefore \quad \boxed{r = \frac{\eta V_T}{I}}$$

The dynamic resistance is inversely proportional to I.

Diode Capacitance :- There are two types of capacitances

i) **Transition capacitance C_T :-** under reverse Bias condition the majority carriers move away from the Junction, thereby uncovering more immobile charges. Hence the depletion region width increases with reverse voltage. This increase in the uncovered charge with applied voltage may be considered as capacitive effect. We may define the

Incremental capacitance $C_T = \left|\frac{dQ}{dV}\right|$

$\therefore \quad dQ = C_T \cdot dV$

$$\frac{dQ}{dt} = C_T \cdot \frac{dV}{dt}$$

$$\boxed{i = C_T \frac{dV}{dt}}$$

The quantity C_T is called as space charge, barrier, depletion region capacitance.

For a reverse biased diode we can prove that

$$\boxed{C_T = \frac{\epsilon A}{w}}$$

Here w = width of the depletion region.

Diffusion Capacitance :- This capacitance is predominant in forward bias. The origin of this larger capacitance lies in the injected charge stored near the junction outside the transition region. It is defined as the rate of change of injected charge with voltage called the diffusion or storage capacitance C_D.

Derivation :- we know that $C_D = \frac{dQ}{dV} = \tau \frac{dI}{dV} = \tau g = \frac{\tau}{r}$

$$\therefore \quad C_D = \frac{\tau}{\eta V_T / I} = \frac{\tau I}{\eta V_T}$$

$$\therefore \quad \boxed{C_D = \frac{\tau I}{\eta V_T}}$$

i.e diffusion capacitance is proportional to I.

Total diffusion capacitance $C = C_{Dp} + C_{Dn}$

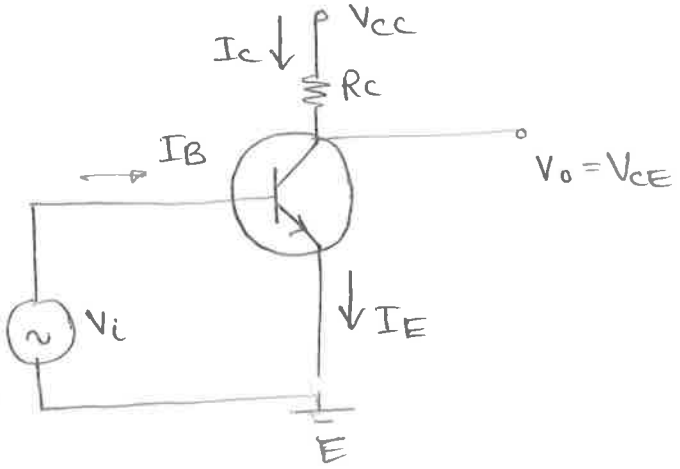
Here C_{Dp} = diffusion capacitance due to holes

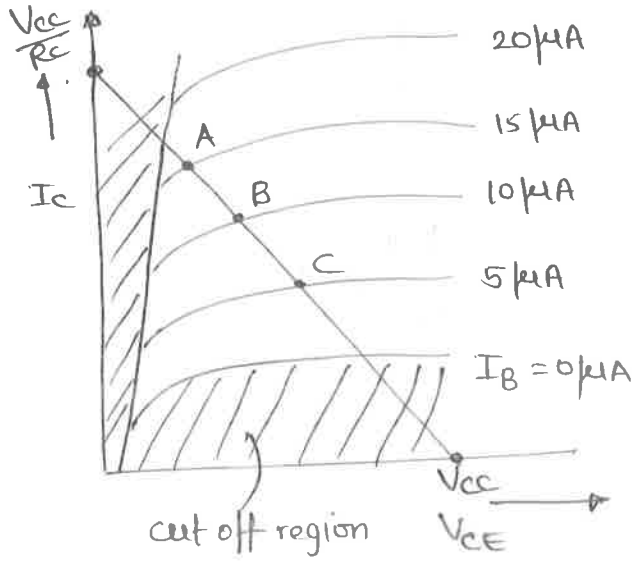
C_{Dn} = diffusion capacitance due to electrons.

Transistor Biasing and stabilization of operating point

Need for Biasing :- The purpose of dc biasing of a transistor is to obtain a certain dc collector current at a certain dc collector voltage. These values of current and voltage are expressed by the term operating point Q. To obtain the operating point we make use of some circuits. and they are called as biasing circuits. For faithful amplification we have to bias the transistors properly.

Selection of operating point Q (V_{CE}, I_C) :- In order to amplify the signal properly the transistor operating point should be fixed properly. The biasing arrangement should be such that the transistor should be active region. Let us take the most popular configuration CE. The common emitter amplifier circuit and its output characteristics are given below.





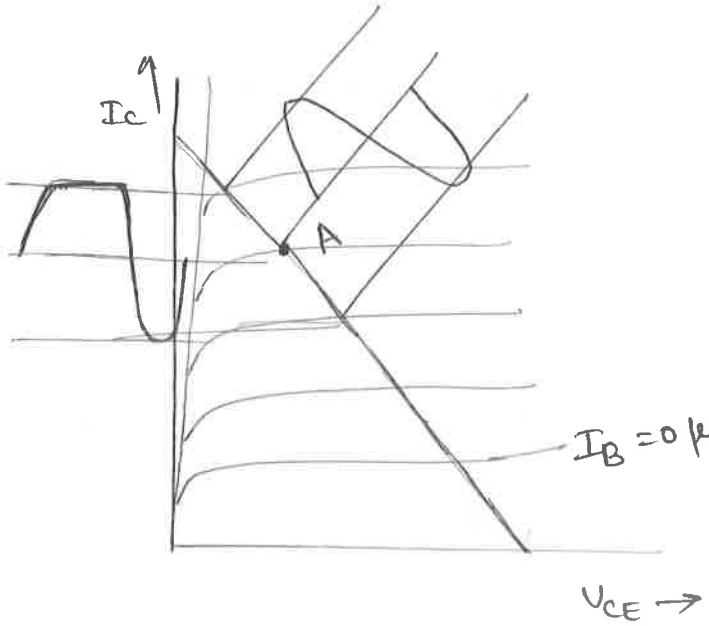
In order to work transistor as an amplifier a load resistance Rc must be connected in the collector circuit. From the output circuit we have $V_{CE} = V_{cc} - I_c R_c$

on x axis $I_c = 0$ $\therefore$ $V_{CE} = V_{cc}$

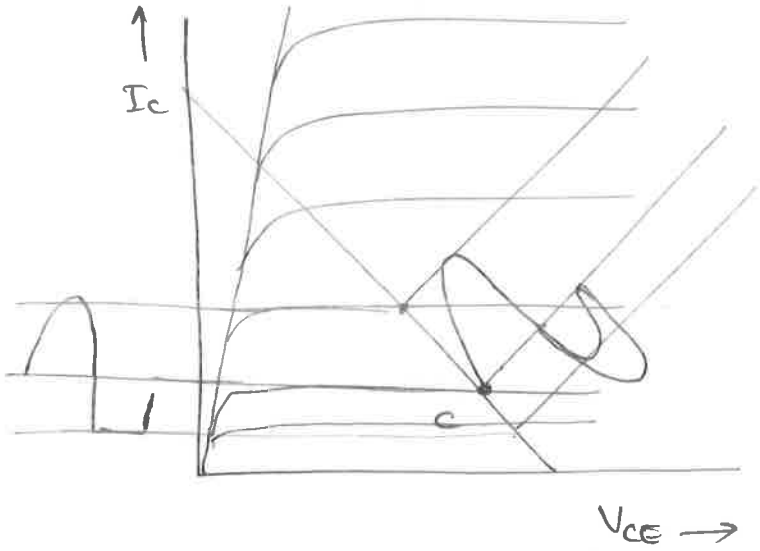
on y axis $V_{CE} = 0$ $I_c = \frac{V_{cc}}{R_c}$

The line connecting the points $(V_{cc}, 0)$ and $(0, \frac{V_{cc}}{R_c})$ is called as Load line

The operating point should ~~on~~ be on this load line either at point A, B or C. For faithful amplification of input signal the best suitable operating point is at B. If the operating point is at A the positive portion of the input is clipped and if it is at C the negative portion will be clipped. as shown in the figure.



The positive portion of the signal is clipped as the operating point Q is at saturation region.



The negative portion of the signal is clipped as the operating point is at cut off region.

Hence the best Location of the operating point is the centre of the Load line. The coordinates of operating point are (V_{CE}, I_C). It is also called as Quiescent operating point or Zero signal point.

Need for Bias stabilization :- Fixing of the operating point is not sufficient. We have to see that it should not move either towards saturation region or cut off region. It must be always in the centre of the Load line. There are two reasons for operating point to shift.

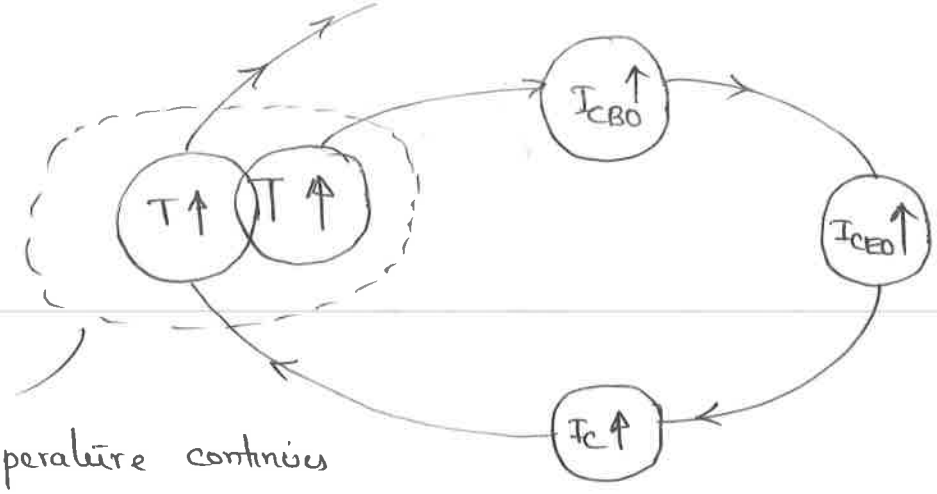
1. The transistor parameters (V_{BE}, I_C, β) are temperature dependent.
2. β value changes from unit to unit.

Flow of current in the collector circuit produces heat at the collector junction. This increases the temperature. More minority carriers are generated in bar collector region. This leakage current I_{CBO} increases.

$$\therefore I_{CEO} = (\beta+1)\, I_{CBO}$$

$$I_C = \beta I_B + I_{CEO}.$$

Thermal Runaway :- It is nothing but the self destruction of a Transistor. The increase in I_{CBO} will cause I_{CEO} to increase, which in turn increases I_C. This further rises the temperature of collector junction and whole cycle repeats again. Such a cumulative increase in I_C will shift the operating point into saturation. This excess heat even burn the transistor. This is called thermal Runaway.

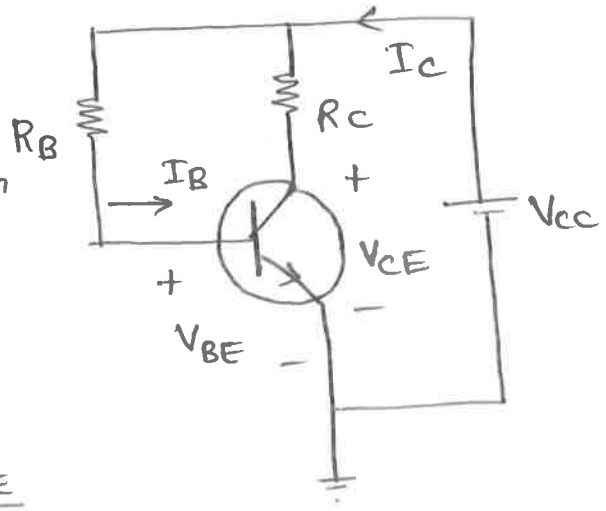


Requirements of a Biasing circuit :-

1. Establish the operating point $Q(V_{CE}, I_C)$ in the centre of Active region.
2. Stabilize the collector current against temp variations
3. Make the operating point (Q) independent of β.

— o —

Fixed Bias :- Fixed Bias circuit is shown below. when I_B flows through the series Resistance R_B, a major portion of the voltage is dropped across it.



Let us consider the input section of the ckt. writing KVL

$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

As V_{BE} is very very less $\boxed{I_B \approx \frac{V_{CC}}{R_B}}$.

As the value of R_B is fixed, I_B is also fixed. Hence it is a fixed bias circuit. $\boxed{I_C = \beta I_B}$

output section :- Considering the output section of the circuit the collector current $I_C = \beta I_B + I_{CEO}$

As I_{CEO} is very small

$$I_C = \beta I_B$$

writing KVL we have

$$V_{CC} = I_C R_C + V_{CE}$$

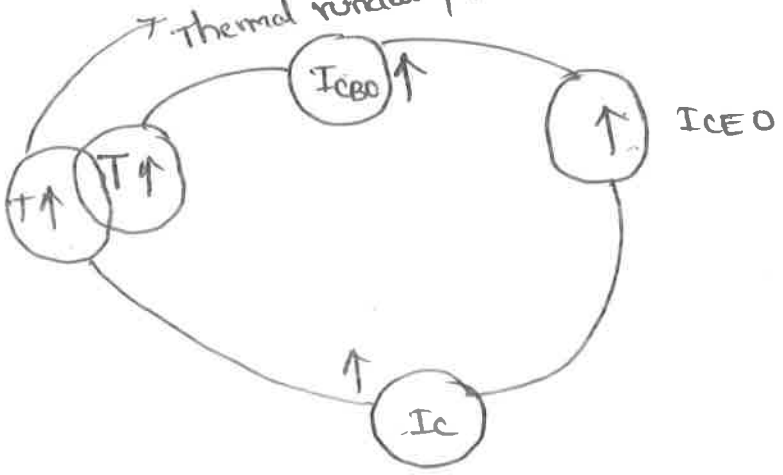
$$V_{CE} = V_{CC} - I_C R_C$$

At saturation $V_{CE} = 0$ $\therefore$ $I_{C(sat)} = \frac{V_{CC}}{R_C}$

$\therefore$ The operating point $Q(V_{CE}, I_C)$ is established.

Advantages :- 1) It is a simple circuit
2) Very easy to establish operating point
3) Few components are used
4) Provides Max flexibility in design.

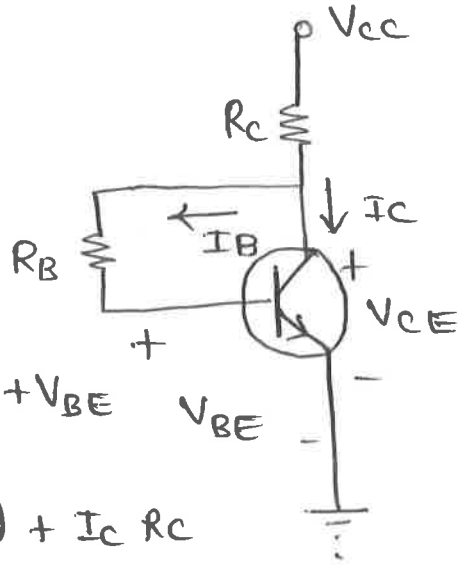
Disadvantage :- 1. Even though it can establish an operating point it fails to stabilize the operating point against temp and β variations



If temp increases I_{CBO} ↑, I_{CEO} ↑ and collector current increase and inturn Temp increase, the transistor enters into thermal runaway.

2. If the transistor is replaced by another transistor, β changes To changes as ($I_C = \beta I_B$) inturn the operating point changes.

Collector - to - base Bias :- The figure shows a modified circuit. Here the base resistor R_B is connected to the collector instead of connecting the supply V_{CC}.



writing the KVL for the input section we have

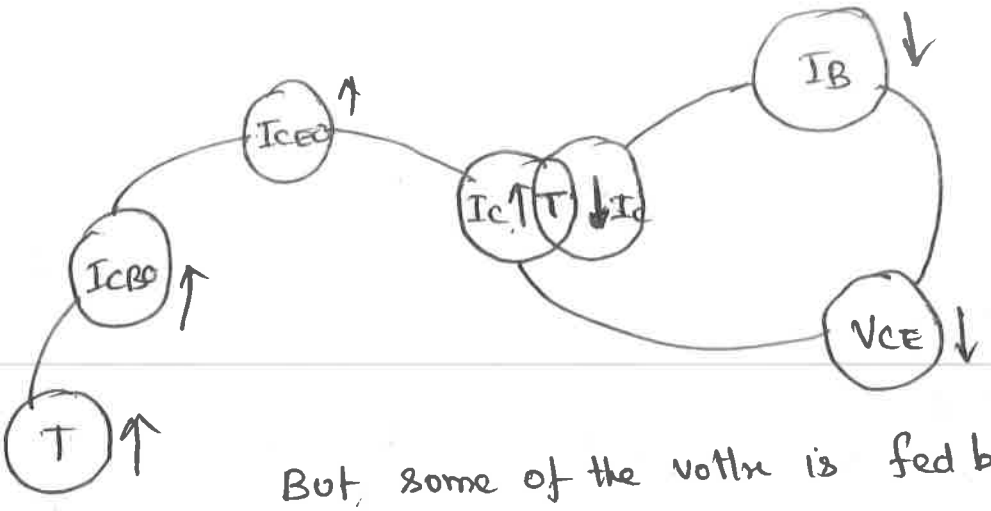
$$V_{CC} = (I_C + I_B) R_C + I_B R_B + V_{BE}$$

$$V_{CC} - V_{BE} = I_B (R_B + R_C) + I_C R_C$$

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_B + R_C} = \boxed{\frac{V_{CE} - V_{BE}}{R_B + R_C}}$$

$$\therefore \boxed{I_C = \beta I_B}$$

If Temp increases, $I_C \uparrow$ and $I_B \downarrow$ and then the output current decreases.



But some of the voltage is fed back to input.

Advantages : i) Easy to establish operating point (Q)

2) control over temp variations

3) coultrol over β variations.

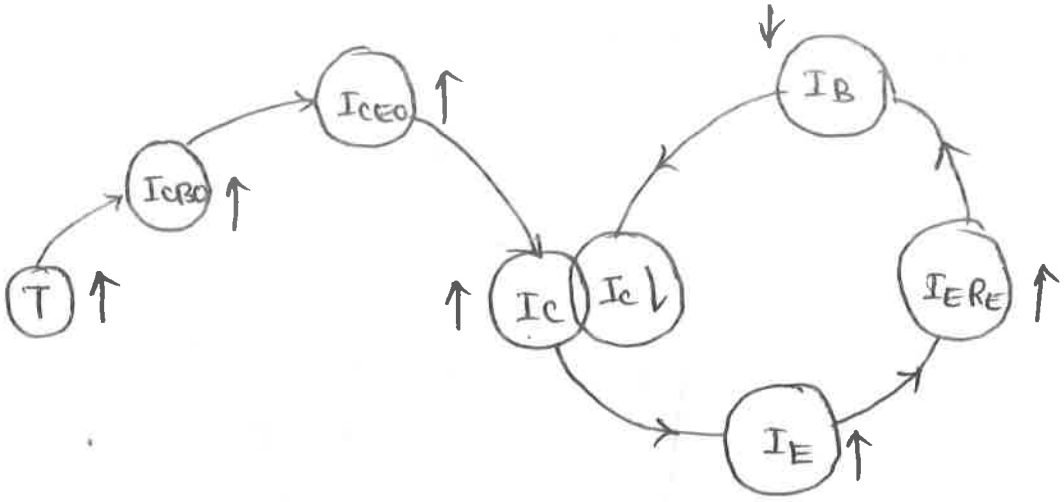
Disadvantage : i) It reduces the voltage gain of an Amplifier

2) It is voltage feedback circuit

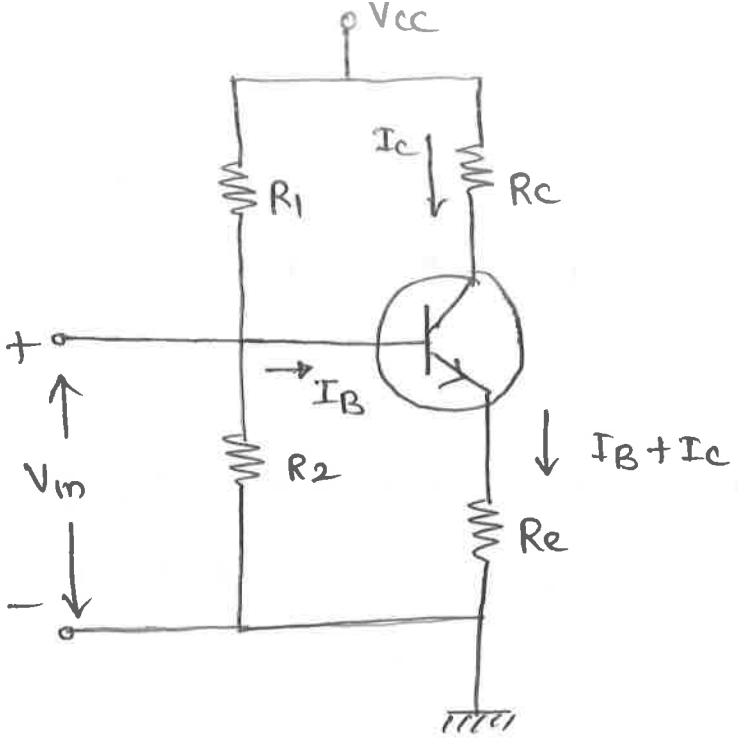
—— o ——

Voltage devider Bias, Emitter Bias, Self Bias :- It is a popular bias circuit which can stabilize the operating point. It has a resistance in the emitter terminal R_e which will reverse bias the emitter junction. As the Biasing is given by voltage division at the base it is called voltage devider Bias.

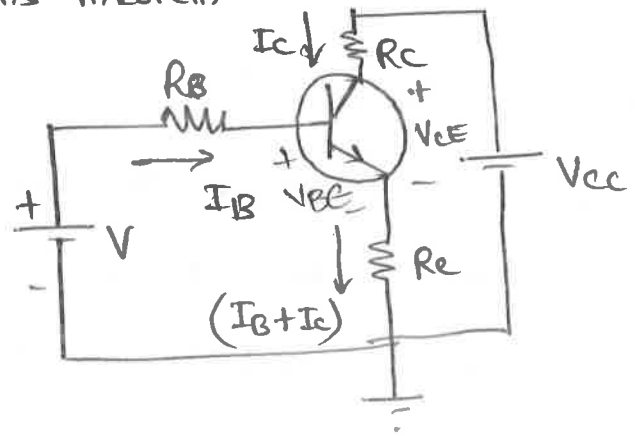
Improvement in stability :-



The voltage across the emitter resistance revers bias the emitter junction, I_B decreases and inturn I_C decreases.



By using Thevinin's theorem we can drawn the above circuit as.



$$V = \frac{V_{cc} \cdot R_2}{R_1 + R_2}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2}$$

Input section : writing KVL we have

$$V = I_B R_B + V_{BE} + (I_B + I_c) R_e$$

$$V = I_B (R_B + R_e) + V_{BE} + I_c R_e$$

$$\boxed{I_B = \frac{V - V_{BE} - I_c R_e}{R_B + R_e}}$$

output section :- $V_{cc} = I_c R_c + V_{CE} + (I_B + I_c) R_e$

$$V_{CE} = V_{cc} - I_c (R_c + R_e) - I_B R_e$$

Advantages : 1) Fixing of operating point is easy.

2). No variation of Q with temperature.

3) No variation of Q with β.

4) Most popular circuit

5) Having so many applications.

Stabilization of operating point Q :- The coordinates of Quiscent operating point is Q (V_{CE}, I_C). The sources of Instability of I_C are three. They are I_{CO}, V_{BE}, β. There are 3 stabilization factors.

Stabilization factor (S) :- It is the rate of change of collector current with respect to reverse saturation current keeping β, V_{BE} const.

$$S = \frac{\partial I_C}{\partial I_{CO}} \approx \frac{\Delta I_C}{\Delta I_{CO}} \text{ at const } \beta \text{ and } V_{BE}.$$

Stability factor (S') :- It is the rate of change of I_C with respect to V_{BE} keeping I_{CO}, β const.

$$S' = \frac{\partial I_C}{\partial V_{BE}} \approx \frac{\Delta I_C}{\Delta V_{BE}} \Bigg| \text{ at const } I_{CO}, \beta.$$

Stability factor (S'') : It is the variation of I_C with β, keeping I_{CO}, V_{BE} constant.

$$S'' = \frac{\partial I_C}{\partial \beta} \approx \frac{\Delta I_C}{\Delta \beta} \text{ at const } I_{CO}, V_{BE}$$

Expression for stability Factor 'S' :- For a common emitter configuration

$$I_C = \beta I_B + I_{CEO}$$

$$I_C = \beta I_B + (1+\beta) I_{CBO}$$

$$\partial I_C = \beta \partial I_B + (1+\beta) \partial I_{CBO}$$

$$1 = \beta \cdot \frac{\partial I_B}{\partial I_C} + (1+\beta) \frac{\partial I_{CBO}}{\partial I_C}$$

$$\left(1 - \beta \frac{\partial I_B}{\partial I_C}\right) = (1+\beta) \cdot \frac{1}{S}$$

$$\boxed{S = \frac{1+\beta}{1-\beta \frac{\partial I_B}{\partial I_C}}}$$

For fixed Bias $I_B = \frac{V_{CC}}{R_C}$

$$\frac{\partial I_B}{\partial I_C} = 0$$

$$\therefore \boxed{S = 1+\beta}$$

Expression for S' :- $I_C = \beta I_B + (\beta+1) I_{CBO}$

$$I_C = \beta \cdot \frac{V_{CC} - V_{BE}}{R_B} + (\beta+1) I_{CBO}$$

$$I_C = \beta \frac{V_{CC}}{R_B} - \beta \frac{V_{BE}}{R_B} + (\beta+1) I_{CBO}$$

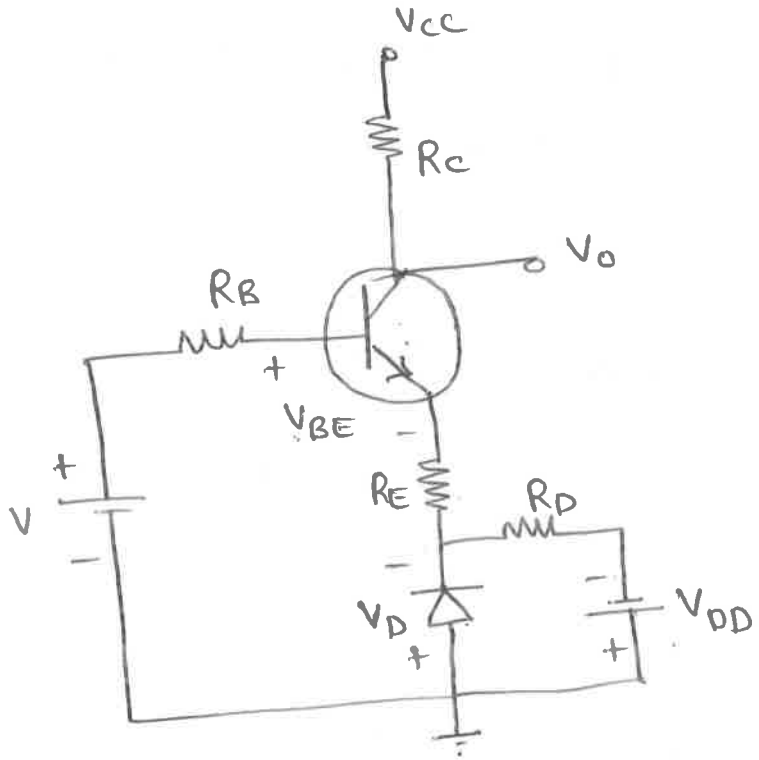
$$\frac{\partial I_C}{\partial V_{BE}} = 0 - \beta/R_B + 0$$

Compensation Techniques.

The stabilization techniques can provide the stability of operating point against the variations of I_{CO}, V_{BE}, β. But due to the feedback of the signals the amplification of the signal decreases. If the loss of amplification is high we go for compensation techniques. Compensation techniques use temp sensitive devices such as diodes, Transistors thermistors and sensistors.

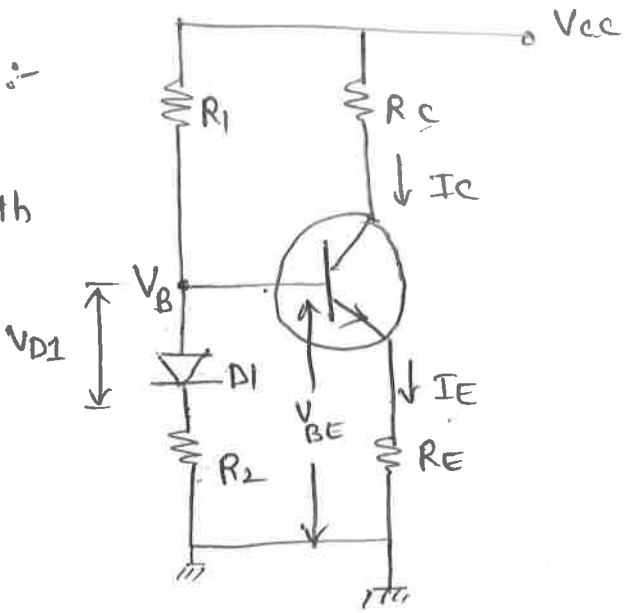
Diode Compensation Techniques :- consider the common Emitter amplifier circuit using voltage devider Bias as shown below.

$$I_C = f(I_{CO}, V_{BE}, \beta)$$



Diode in emitter circuit :- Here the supply V_{DD} is used to forwardbias the diode. The material used for diode is same as Transistor. The change in V_{BE} with temperature will be compensated by the change in Diode and hence the they tend to cancel each other. The diode has the same temp coefficient as that of the base to emitter voltage V_{BE}.

b) Diode in voltage devider circuit :-



The diode is connected in series with the resistor R_2. in the forward biend coudution.

$$I_E = \frac{V_B - V_{BE}}{R_E}$$

$$I_C = \frac{V_B - V_{BE}}{R_E}$$

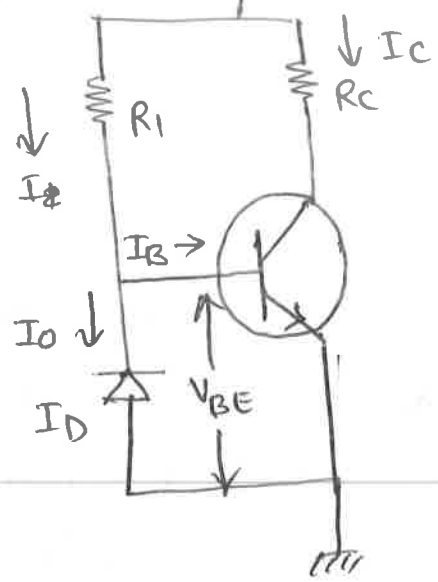
$$I_C = \frac{V_{R_2} + V_D - V_{BE}}{R_E}$$

If V_{BE} changes with temperature V_D also changes in a direction opposite to the change of V_{BE}. Then the collector current is independent of those.

$$I_C = \frac{V_{R_2}}{R_E}$$

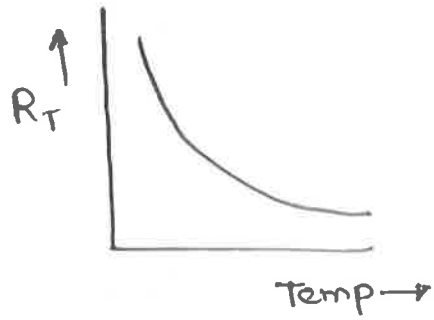
Diode and transistor materials are of the same type.

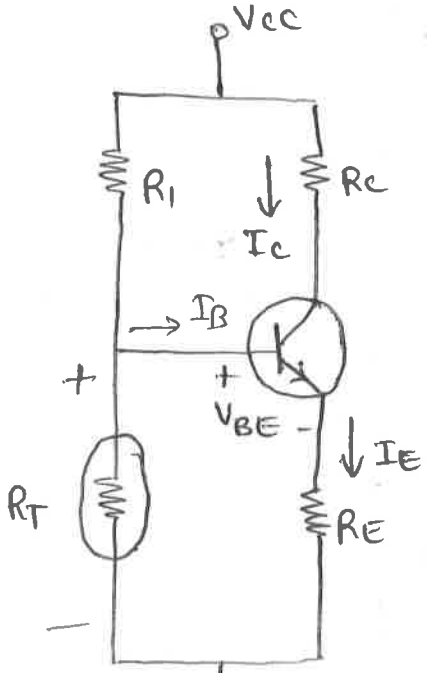
c) compensation against vanation in I_{CO} :-



The diode is reverse biand and leakage current flows through the diode. If the diode and Transistor of the same material the current I_o increase with temp at the same rate as the collector leakage current I_{CO}.

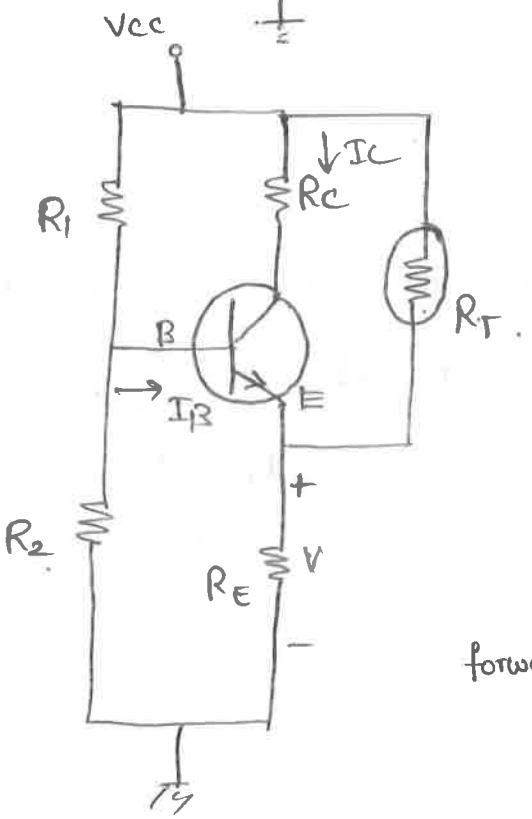
Thermistor compensation :- Thermistor has a negative temperature coefficient i.e resistance decreases exponentially with temperature.





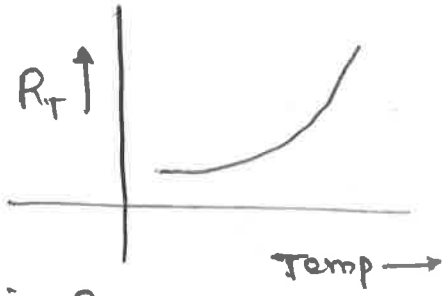
Here R_2 is replaced by R_T (Thermistor).

If Temperature increases R_T decreases Hence the voltage drop across R_T decreases and hence forward biasing is decreased. Then the input current I_B reduces. The output current will be controlled.

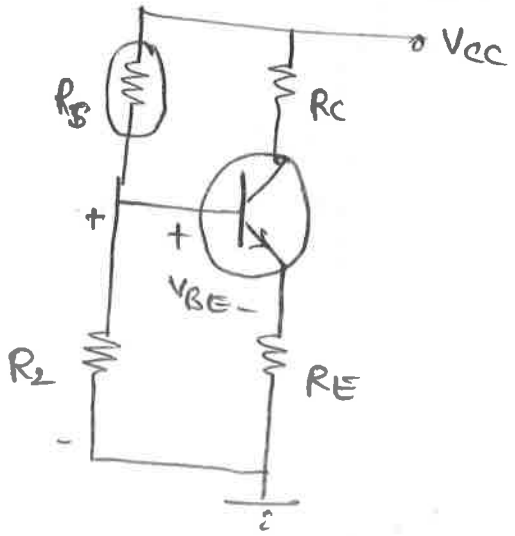


If temperature increases I_C increases but R_T decreases. Then current flowing through R_E increases, which increases the voltage drop across R_E and reduces the forward biasing on B-E junction. Then the input current decreases and inturn output current is controlled.

Sensistor Compensation :- Sensistor has +ve temperature coefficient of resistance. The resistance increases exponentially with temperature.



The sensistor is placed in the position R_1 as shown in the figure.



$T \uparrow \; I_C \uparrow$

$R_S \uparrow \; V_{R_2} \downarrow \; I_B \downarrow \; I_C \downarrow$

As the Temperature increases R_S increases which decreases the current flowing through it. Then the voltage across R_2 decreases and forward biasing is decreased. Then the input current decreases and in turn output current I_C decreases.

– o –

Thermal Runaway :- It is to be noted that heat always will be dissipated at the collector Junction. The collector base Junction temperature may rise because of two reasons.

a) Due to rise in ambient temperature

b) Due to self heating.

The increase in the collector current increases the power dissipation at the collector Junction. Then it increases temperature of the Junction and in turn collector current I_C. This cumulative process is called as self heating. The excess heat evolved at the Junction destroy the transistor. Thus the self destruction of Transistor due to temperature is called as "Thermal Runaway".

Thermal Resistance : The steady state temperature at the collector Junction is proportional to power dissipated at the Junction.

$$T_J - T_A = \theta P_D$$

T_J = Junction temperature

T_A = Ambient "

θ = Thermal Resistance.

Thermal stability :

To avoid the thermal Runaway the required condition is

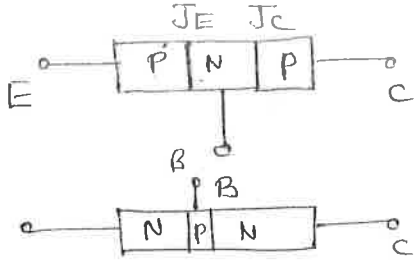
$$\frac{\partial P_C}{\partial T_J} < \frac{\partial P_D}{\partial T_J}$$

i.e the rate at which the heat is released must be less than

Transistors - characteristics.

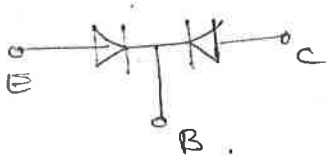
UNIT-5

Transistor → Transfer + Resistor.



3 layers, 3 terminals & two Junction device

Back to Back connection of two diode



Emitter : which emits charge carriers

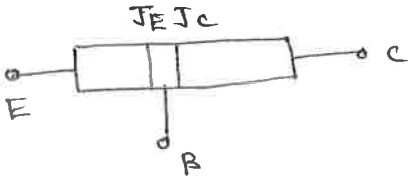
: Heavily doped.

: Medium Size

Base : controlling the carriers, lightly doped, Very thin

collector : which collects the carriers emitted from emitter

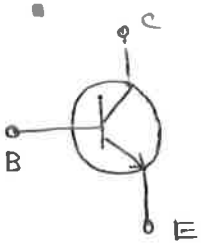
: Large size, Medium doping



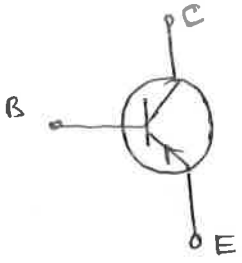
Regions of Transistor :

	J_E	J_C	Region
*	FB	RB	Active Region → Amplifier.
	FB	FB	Saturation Region → DE (0)
	RB	RB	cut off Region → DE (1)
	RB	FB	Inverse Active Region → No application

Symbols of Transistors :

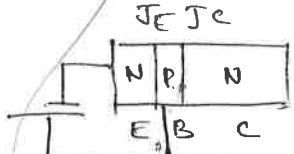


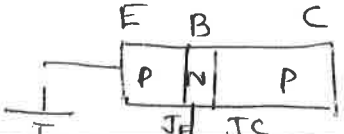
NPN.



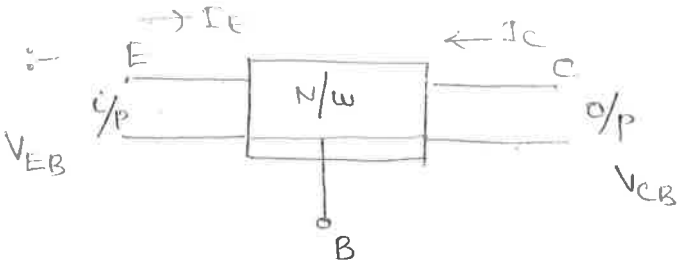
PNP.

Arrow indicates the direction of the current when J_E is forward Biased.

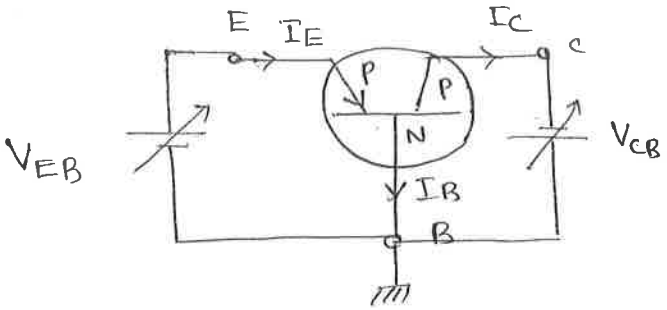




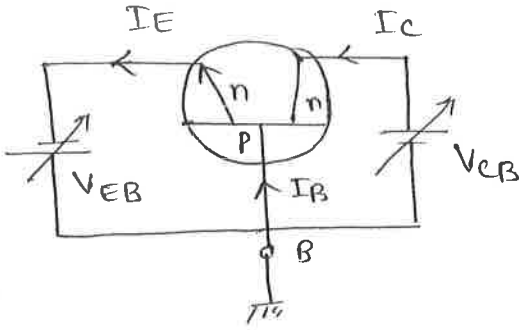
Different configurations :-



CB configuration : Base is common for both i/p and o/p.



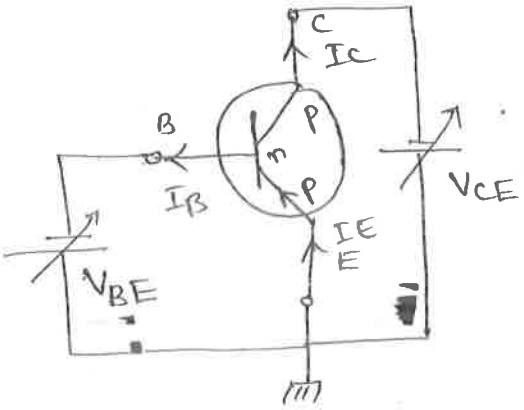
CB (PNP)



CB using (NPN)

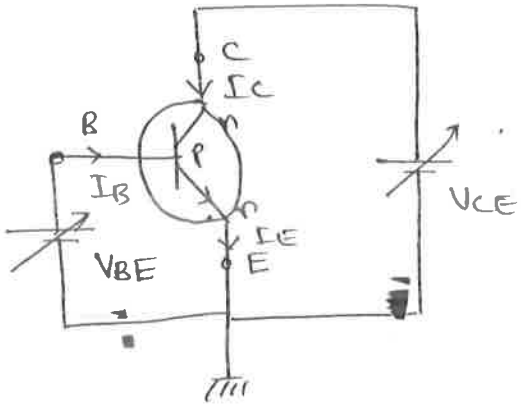
$$I_E = I_B + I_C$$

CE configuration : Emitter is common for both i/p and o/p.



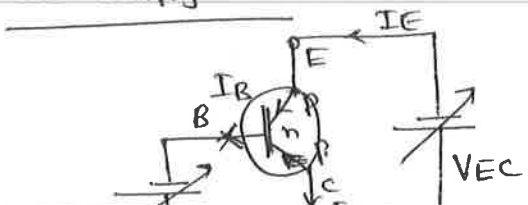
$I_E = I_B + I_C$

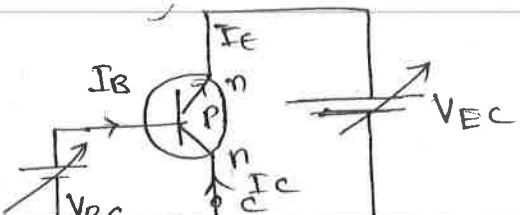
CE. using (PNP)



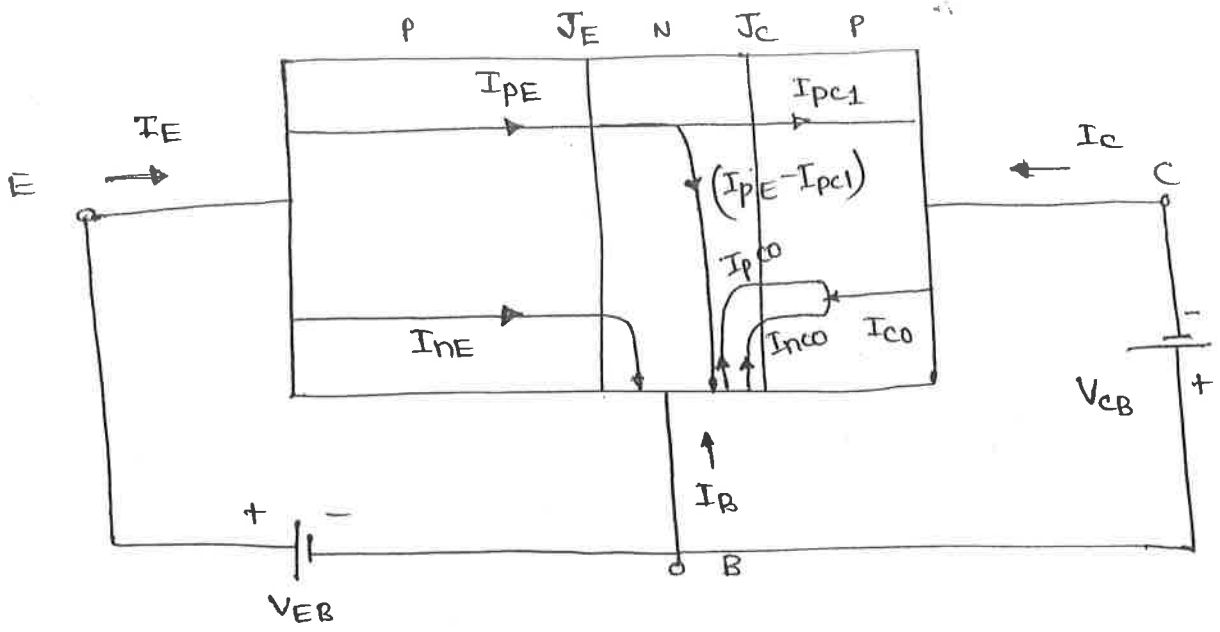
CE using (NPN)

CC configuration : collector is common for both i/p and o/p.





Transistor current components :-



In the above figure we have shown different types of currents which flow across the forward biased emitter junction and reverse biased collector junction. The emitter current I_E consists of hole current I_{PE} i.e due to holes crossing from emitter junction and I_{nE} due to crossing of electrons from base to emitter.

$$\therefore I_E = I_{PE} + I_{nE}$$

As the doping of emitter is very high we have $I_{PE} \gg I_{nE}$

$$\therefore I_E \approx I_{PE} \text{ (i.e due to holes)}$$

All the holes crossing the emitter junction does not reach to the collector as recombination takes place in the base region. Let I_{pc1} represents the hole current reaching to the collector. i.e there is recombination current $(I_{PE} - I_{pc1})$ in the base region.

At the collector Junction there a leakage current across the Junction due to reverse bias. The reverse current consists of I_{pco} and I_{nco}

$$\therefore \boxed{-I_{co} = I_{pco} + I_{nco}}$$

The total collector current

$$I_C = I_{co} - I_{pc1} = I_{co} - \alpha I_E$$

Large signal current gain α :- It is defined as the ratio of -ve of the collector current increment from cut-off and emitter current.

$$\alpha = -\left(\frac{I_C - I_{co}}{I_E - 0}\right)$$

Alpha is called as the large signal current gain of CB amplifier.

combining the currents at J_E and J_C the total Transistor current equation is

$$I_C = -\alpha I_E + I_{co}\left(1 - e^{V_c/V_T}\right)$$

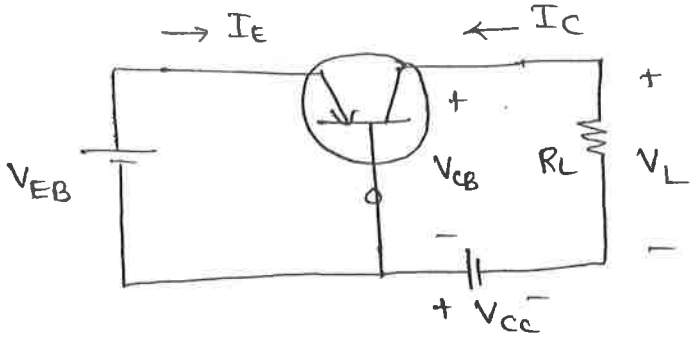
Emitter efficiency (γ) :- It is the ratio of current due to diffusion of holes at the emitter junction to the total current (I_E)

$$\boxed{\gamma = \frac{I_{pE}}{I_{pE} + I_{nE}} = \frac{I_{pE}}{I_E}}$$

Bax Transportation factor (β) :- It is the ratio of current reaching to the collector to the total emitter current.

$$\boxed{\beta = \frac{I_{pc1}}{} = \frac{I_{pc1}}{}}$$

Transistor as an Amplifier :- Let us explain this concept by taking PNP Transistor operating in the active region in CB configuration.



A load resistance R_L is placed in series with the supply voltage V_{CC}.

A small change in ΔV_i causes large change in input current ΔI_E

Then the change in collector current $\Delta I_C = \alpha' \Delta I_E$. The output voltage is

$$\Delta V_L = -R_L \Delta I_C = -\alpha' R_L \Delta I_E \quad \text{— (1)}$$

The dynamic resistance of the emitter junction is r_e

$$\Delta V_i = r_e \cdot \Delta I_E \quad \text{— (2)}$$

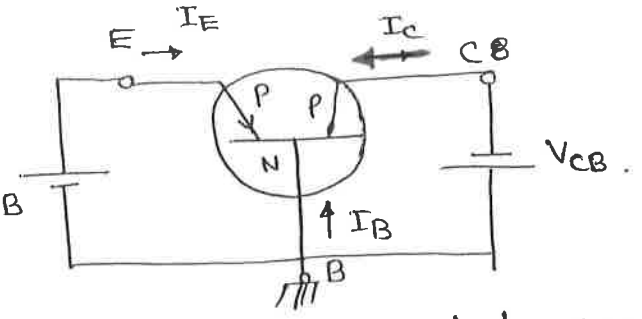
Then gain $A = \dfrac{\Delta V_L}{\Delta V_i} = \dfrac{-\alpha' R_L \Delta I_E}{r_e \Delta I_E}$

$$\boxed{A = -\alpha' \frac{R_L}{r_e}} \qquad r_e = \frac{26}{I_E}$$

The parameter (α') :- It is the ratio of the change in the collector current to the change in the emitter current at constant collector to base voltage

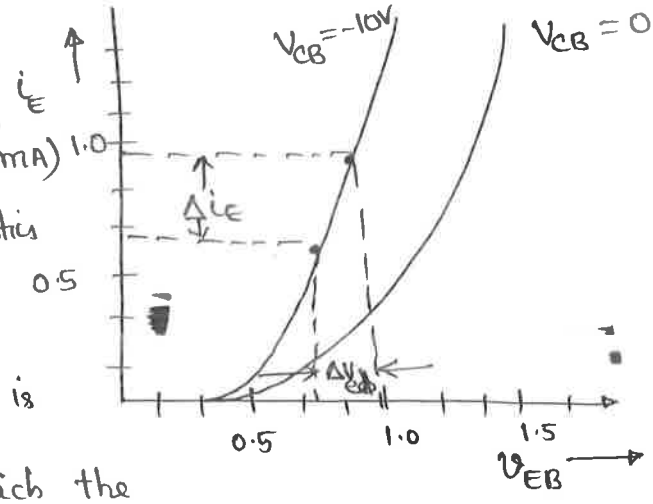
$$\boxed{\alpha' \equiv \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB}}}$$

Common Base configuration :- In this configuration base is common for both input and output common Base configuration is given using PNP Transistor. There are two sets of characteristics which describe completely the operation of a transistor in static mode. one is the input characteristics and other is the output characteristics.



The transistor is operated in the active region in which Emitter Junction is forward biased and collector junction is reverse Biased. Here I_E is positive and I_B, I_C are negative. V_{EB} is positive and V_{CB} is -ve. All these polarities will be reversed for NPN Transistor.

Input characteristics :- It is the graph plotting between V_{EB} and i/p current I_E keeping output voltage V_{CB} constant. The following graph indicates input characteristics for PNP in CB configuration.

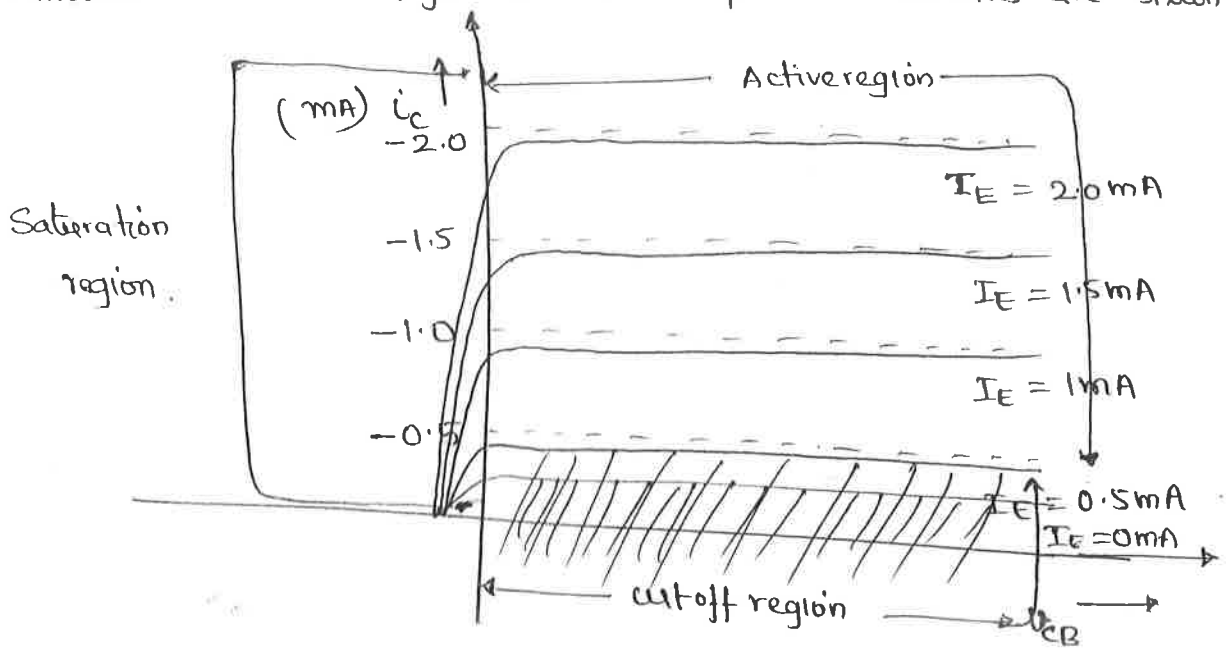


As the transistor consists of two diodes placed in series "back to back" the input characteristics simply same as the diode characteristics. Here also there is a cutin voltage V_r below which the emitter current is zero. From these characteristics we can find the dynamic input resistance of a Transistor.

$$r_i = \left.\frac{\Delta V_{BEB}}{\Delta I_E}\right|_{V_{CB}=\text{const}}.$$

The dynamic input resistance is Very low (upto 100 Ω)

Output characteristics :- It is the graph plotting between output voltage (V_{CB}) and output current (I_C) keeping input current (I_E) constant. For the same PNP Transistor in CB configuration the output characteristics are shown below.



From the above characteristics we can conclude the following points

1. The collector current is approximately equal to the emitter current. This is true in the active region.
2. In the active region the curves are almost flat. i.e i_C increases slightly with V_{CB}. Hence CB configuration can be used as const current source.

The total characteristics are well explained by dividing into 3 regions.

i) cut off region : It is the region in which emitter junction is ~~forward~~ Reverse Biased and collector junction is also reverse Biased. i.e both junctions are reverse Biased. The region below $I_E = 0mA$ is the cutt off region of Transistor in CB configuration. In this region a small reverse saturation current flows through the transistor I_{CBO}.

ii) Saturation Region :- The region to the left of ordinate $V_{CB} = 0$

forward Biased is called the saturation region. In this region collector current does not depend much on the emitter current.

Active region :- In this region J_E is forward biased and J_c is reverse biased. In this region the collector current I_c independent of output voltage V_{CB} and depends only upon emitter current. In this region this configuration can be used as a constant current source.

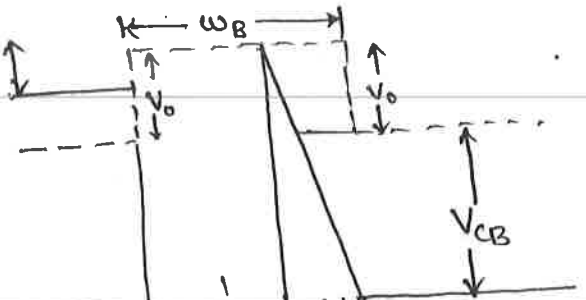
From the output characteristics we can find the output dynamic resistance

$$r_o = \left.\frac{\Delta V_{CB}}{\Delta i_c}\right|_{I_E = \text{constant}}$$

The current gain (α) is defined as the ratio of collector current to emitter current $\therefore \alpha = \frac{I_c}{I_E} \quad (I_c \approx I_E)$

The value of α is less than unity and typical value is 0.98.

Early Effect or Base width Modulation :- whenever the transistor is operated in the active region the depletion region width at J_E decreases due to forward Bias and the depletion region width at J_c increases due to Reverse Bias. The depletion region width increased with V_{CB} and increases more towards Base compared to collector side. This is due to the light doping of the base region. The depletion region widths are shown below.



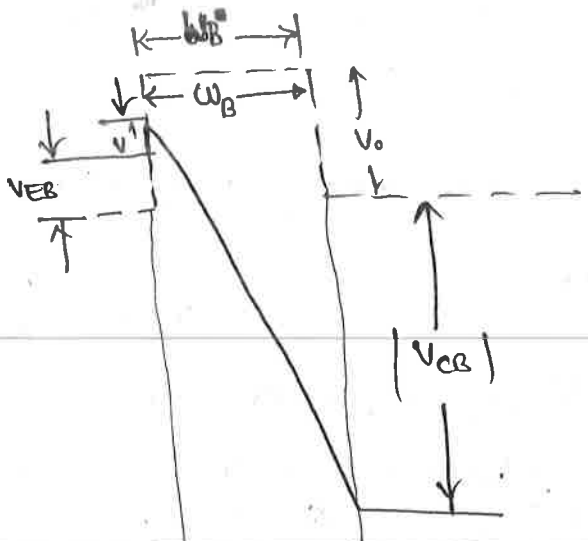
If the metallurgical base width is W_B the effective electrical base width is

by collector voltage V_{CB} is known as Early effect. If we go on increasing V_{CB}, W_B' may be reduced to zero causing the voltage break down in the Transistor. This phenomenon is known as Punch-through

- Break down Mechanisms in a Transistor :-

a) Punch through (Reach-through) :- It is the Mechanism by which transistor's usefulness may be terminated as the collector voltage is increased is called punch through or reach through. This effect is due to the increased width of the collector junction transition region with increased collector junction voltage.

As the voltage applied across the junction increases, the transition region penetrates deeper into base. Since the base is very thin at moderate voltages the transition region will have spread completely across the base to reach the emitter junction. The emitter barrier is now V', which is smaller than the normal value $V_o - |V_{EB}|$ because the collector voltage has reached through the base region.



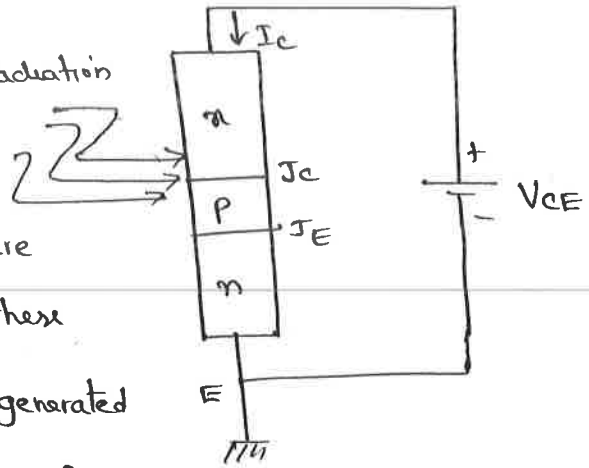
Avalanche Multiplication :- The Maximum reverse-biasing voltage which may be applied before breakdown between the collector and base terminals of the transistor, under the condition that the emitter lead be open circuited is represented by the symbol BV_{CBO}. Breakdown is due to avalanche multiplication of the current I_{CO} that cross the collector junction. As a result of this multiplication the current becomes MI_{CO} in which M is the factor by which the original current I_{CO} is multiplied by avalanche effect.

The avalanche Multiplication factor depends on the voltage V_{CB}

$$M \equiv \frac{1}{1 - \left(\frac{V_{CB}}{BV_{CBO}}\right)^n}$$

— o —

The photo Transistor :- The photo Transistor is also called as photodiode. It is much more sensitive semi conductor device than the photo diode. The photo transistor is generally connected in common Emitter configuration with the base open. Radiation is concentrated on the region near collector junction J_c. The photo transistor is given below.



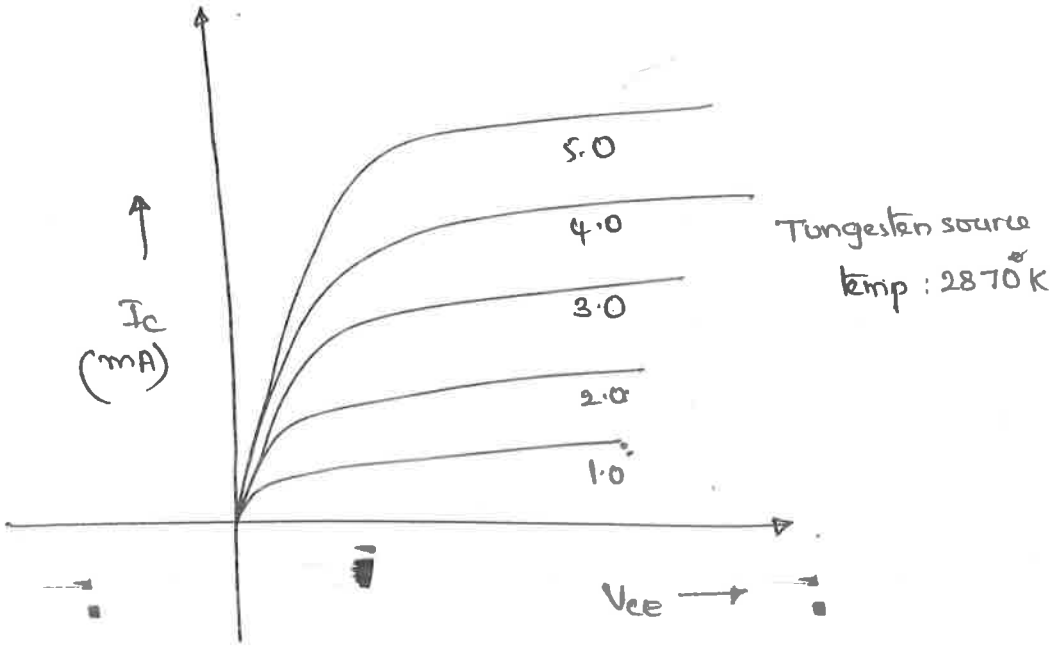
Operation : The emitter junction is slightly forward biased and J_c is reverse biased. Assume that there is no radiation initially. under these circumstances minority carriers are generated thermally and the electrons crossing from

constitute reverse saturation current I_{CO}. The collector current is given by $I_C = (\beta+1) I_{BCO}$ $(I_B = 0)$

If the light is now turned ON, additional minority carriers are photogenerated and they contribute to the reverse saturation current. If the component of reverse saturation current due to light is I_L, the total collector current is

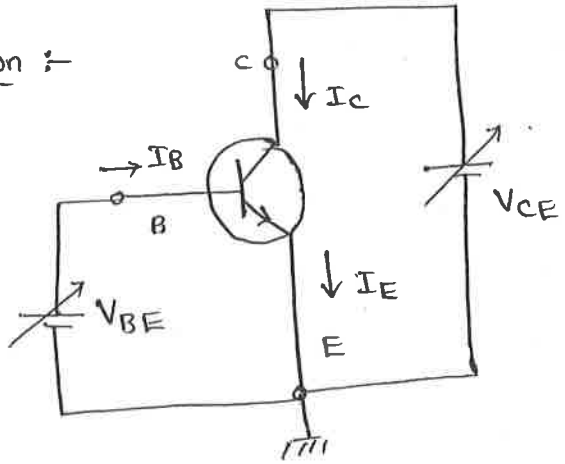
$$I_C = (\beta+1)(I_{CO} + I_L)$$

The typical Volt-ampere characteristics of photo transistor is given below.



The above characteristics are for an n-p-n planar phototransistor for different values of illumination intensities.

CE configuration :- In this configuration the emitter is made common to the input and the output. The signal is in between base and emitter and the output is in between collector and emitter. The transistor is operated in the active region. The transistor is npn type and CKT is shown below.



Current Relations in CE configuration :-

we know that $I_E = I_B + I_C$

$$I_C = \alpha I_E + I_{CBO}$$

$$I_C = \alpha (I_B + I_C) + I_{CBO}$$

$$(1-\alpha) I_C = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$

$$\boxed{I_C = \beta I_B + I_{CEO}}$$

Here $\beta = \frac{\alpha}{1-\alpha}$ & $I_{CEO} = \frac{1}{1-\alpha} I_{CBO}$

It is evident that the reverse saturation current in CE is more than CB. The factor β is called as common emitter DC current gain.

If I_{CEO} is very small compared to I_C then :

$$\boxed{\beta = \frac{I_C}{I_B}}$$

Relation between α and β :-

$$\beta = \frac{\alpha}{1-\alpha}$$

$$\beta - \alpha\beta = \alpha$$

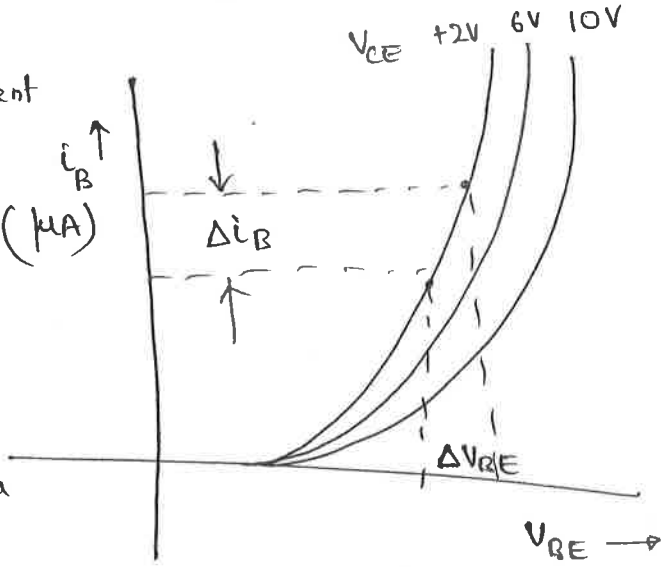
$$\frac{I_E}{I_C} = \frac{I_C}{I_C} + \frac{I_B}{I_C}$$

$$\frac{1}{\alpha} = 1 + \frac{1}{\beta}$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

Input CE characteristics :- It is graph between input voltage (V_{BE}) and Input current (I_B) keeping output voltage V_{CE} constant.

The curves are drawn for different values of V_{CE}. Note that the output voltage V_{CE} does not result in a large deviation of the curves.



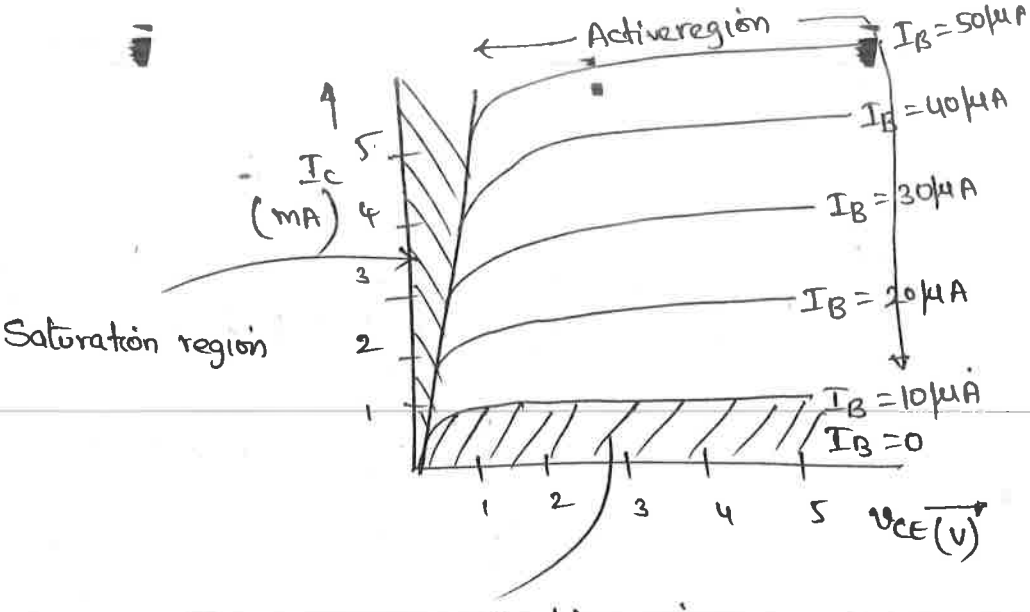
The Input dynamic resistance of a transistor is

$$r_i = \frac{\Delta V_{BE}}{\Delta i_B}$$

$$r_i = \frac{\Delta V_{BE}}{\Delta i_B}.$$

As i_B is very less the input resistance is high.

output characteristics :- It is graph between ~~very~~ output voltage (V_{CE}) and output current I_C keeping input current constant. For an npn transistor V_{CE}, I_C and I_B are all positive. The output characteristics are given below.



Active Region :- It is the region in which emitter junction is forward biased and collector junction is reverse Biased. In this region i_c increases slowly as V_{CE} increases. The slope of these curves is some what greater than CB output characteristics. In the figure the active region is the area to the right of the ordinate V_{CE} = a few tenths of a volt and above $i_B = 0$. If the transistor is to be operated as an Amplifier it must be biased in this region. In this region

$$I_C = \beta I_B + \frac{1}{1-\alpha} I_{CO}$$

$$\boxed{I_C = \beta I_B + (\beta+1) I_{CO}}$$

Saturation Region :- If V_{CE} falls below a few tenths of volt, i_c decreases rapidly as V_{CE} decreases. This occurs as V_{CE} drops below the value of V_{BE} the collector-base junction becomes forward Biased. In this condition both junctio are forward biased. The transistor is working in the saturation region. as the emitter current I_C no longer depends upon the input current i_B. It is shown in the graph.

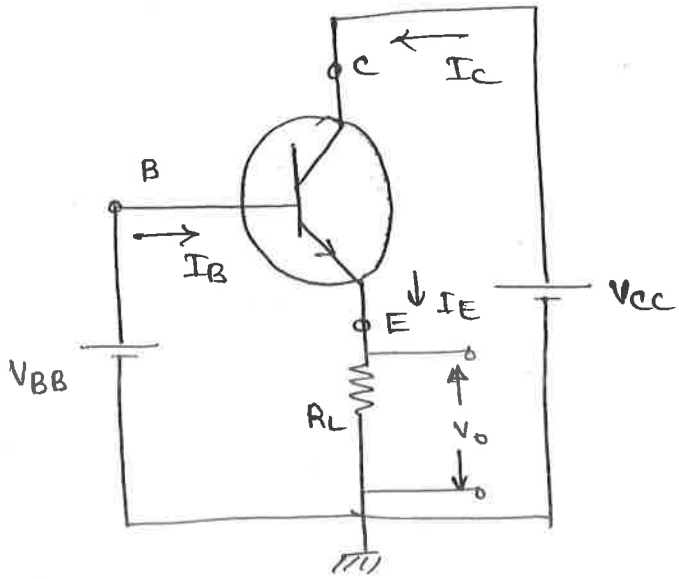
Cut off Region :- It is the region in which both junctions are reverse biased when the collector junction is reverse biased a small amount of leakage curren I_{CEO} flows through the transistor even though $i_B = 0$. This reverse Leaka current is more in CE compared to CB.

$$I_{CEO} = \frac{1}{1-\alpha} I_{CBO}$$

Common collector configuration :— In this configuration collector is common for both input and output. It is exactly like a CE circuit except for the fact that the output is taken at the emitter rather than collector. The Load Resistance R_L is connected between the emitter and the ground. This circuit is also called as "Emitter Follower".

Current gain

$$\gamma = \frac{I_E}{I_B}$$



Current Relations in CC configuration :— In this configuration the output current is function of Input current i.e $I_E = f(I_B)$

$$I_E = I_B + I_C$$

$$I_C = \alpha I_E + I_{CBO}$$

$$I_E = I_B + \alpha I_E + I_{CBO}$$

$$(1-\alpha) I_E = I_B + I_{CBO}$$

$$I_E = \frac{1}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$

$$I_E = (\beta+1) I_B + (\beta+1) I_{CBO}$$ If I_{CBO} is neglected then

$$I_E = (\beta+1) I_B$$

Comparision between CB, CE, CC configurations.

S.NO.	parameter	CB	CE	CC
1.	Input dynamic resistance (r_i)	Very low 20Ω	Low (1KΩ)	very high
2.	O/p dynamic Resistance (r_o)	Very High (1MΩ)	High (10KΩ)	High
3.	current gain	Less than unity $\alpha = \frac{I_C}{I_E}$ (0.98)	High (100)	Very High.
4.	Leakage current	Very small I_{CBO}	Very large	Same as CE
5.	Applications	Const current source	Amplifiers	Darlington ckt. Buffer ckt

Why CE configuration is popular :-

1. The main application of Transistor is as an amplifier. Sometimes as a single stage is not sufficient we have to use multistages - when ever more stages are connected in cascade we have to see that one stage should not load the other stage. So For this purpose CE configuration is more preferable due to its excellent qualities like

   i) High Voltage gain (A_V)

   2) High current gain (A_I) (obviously power gain is also high) $A_p = A_V A_I$

   3) High Input resistance

   4) Low output Resistance

UNIT - 6

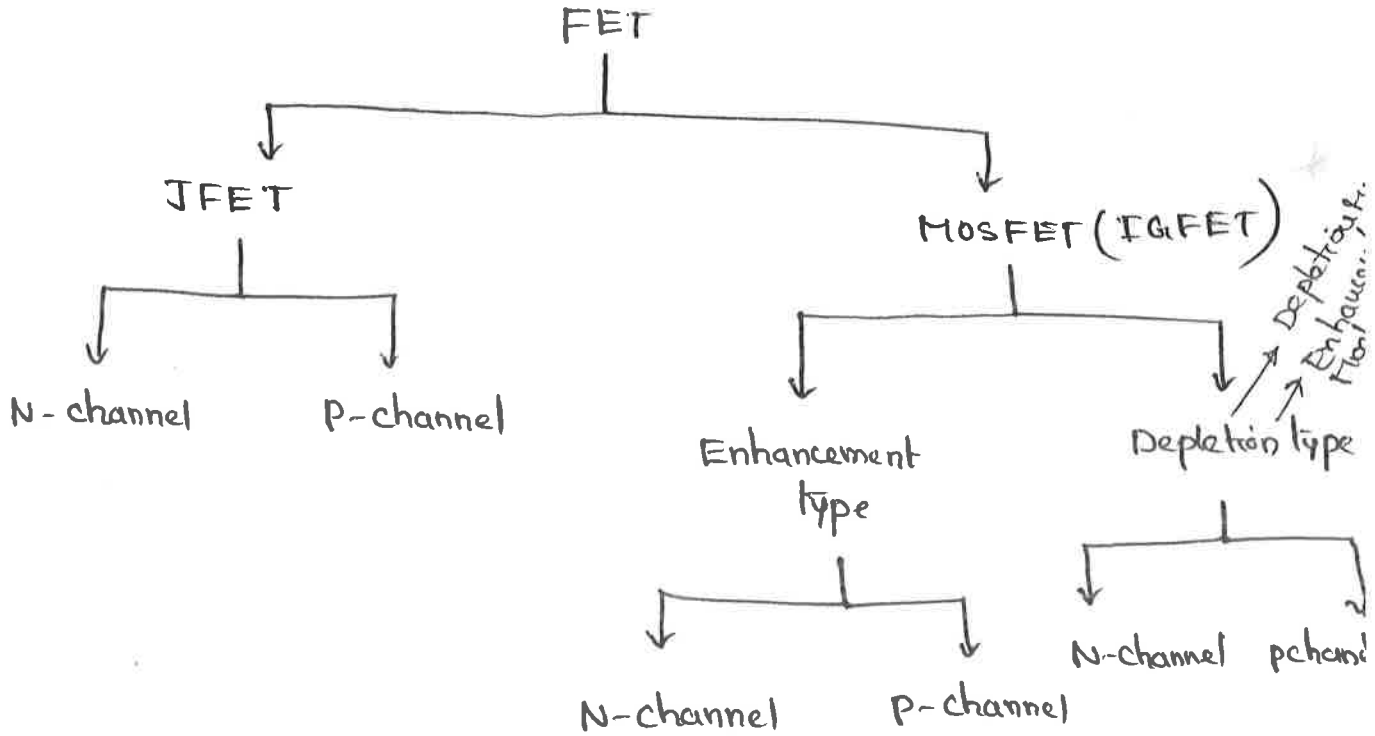
Differences between BJT and JFET

FET	BJT
1. It is a unipolour device (i.e.) Current in the device is either by electrons or holes.	1. It is a bipolar device i.e. current in the device is carried by both electrons and holes.
2. It is a voltage Controlled device (i.e) voltage at the gate terminal controls the amount of current through the device.	2. It is a current controlled device (i.e.) the base current controls the amount of collector current.
3. Input resistance is very high and it is in the order of mega ohms.	3. Input resistance is very low as compared to FET and is of order of few ohms to KΩ.
4. It has negative temperature coefficient, it means that current decreases as the temperature increases. This, characteristic prevents the FET from thermal breakdown.	4. It has a positive temperature coefficient. This characteristic leads BJT to thermal breakdown.
5. It does not suffer from minority carrier storage effects and it has higher switched speeds and cut off frequencies.	5. It suffers from minority carrier storage and it has lower switching speed and cut off frequencies that of FET's.
6. It is less noisy.	6. More noisy than a FET.
7. Simpler to fabricate as a IC and occupies a less space on IC.	7. Difficult to fabricate as an IC and occupies more space than that of FET.
8. Cost is high.	8. Cost is low.

Field Effect Transistor (FET)

The Field effect Transistor developed in 1960. The advantages of FET over the Junction Transistors are that they have high input impedance and high power gain. FETs are comparatively easier to fabricate. Fet is called as Unipolar device as it's current is only due to Majority carriers i.e only due to one type of carriers. As the drain current is controlled by the field. It is called as Field effect Transistor.

Classification of FETs :-



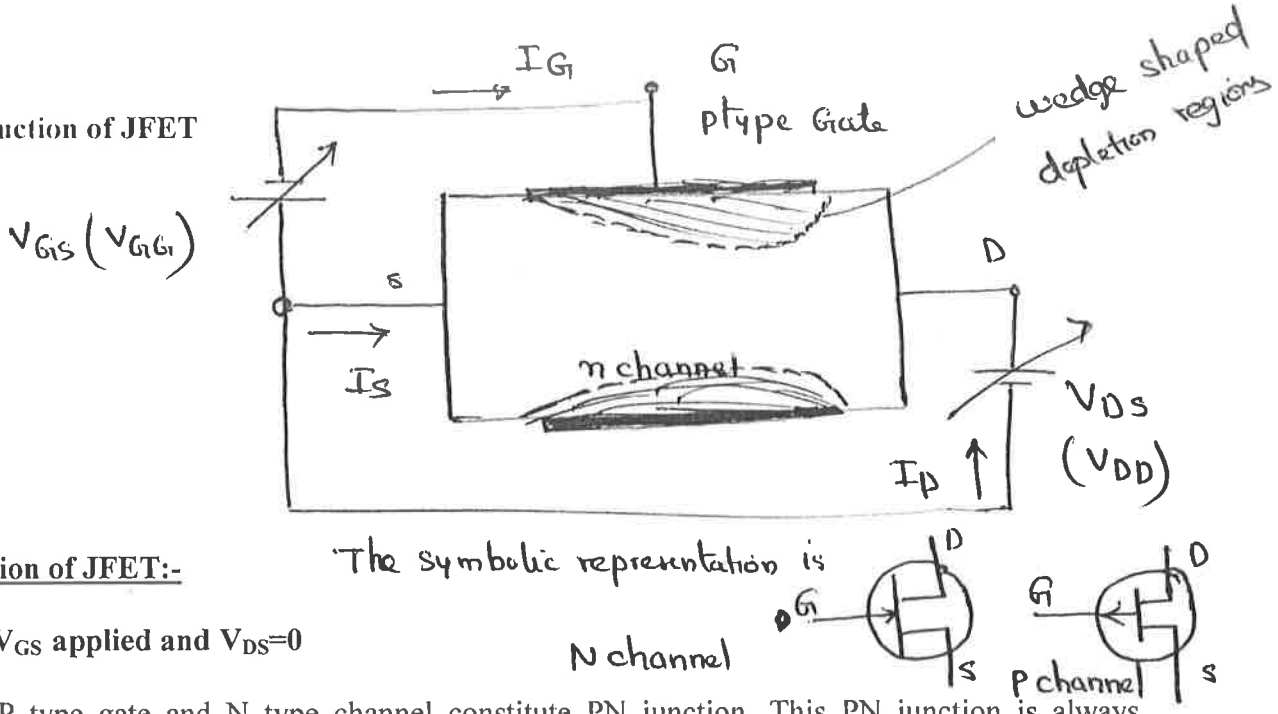
Junction Field Effect Transistor :- The structure of n channel FET is shown in the figure. It is an n-channel Fet where the current is due to electrons only. This bar behaves like a resistor between the two terminals called source and drain. There are 3 terminials in the JFET.

a) Source : It is a terminal through which majority carriers enter into the bar.

b) Drain : It is the place where the majority carriers leave the bar.

c) Gate : On both sides of N type bar heavily doped p. regions are

Construction of JFET



Operation of JFET:-

The symbolic representation is

When V_{GS} applied and V_{DS}=0

- P type gate and N type channel constitute PN junction, This PN junction is always reverse biased in JFET operation.
- The input junction Gate and source always reverse biased by using V_{GG} (V_{GS}) supply. whenever it is in the reverse bias condition electrons and holes diffuse across the junction leave behind positive and negative ions on N-side and P-side, and these ions are immobile ions, is known as "depletion region".
- When P and N regions are heavily doped, the depletion region extend symmetrically on both sides, but 'P' region is heavily doped than N type channel, thus depletion region extents more in N-region than the P-region.
- When no V_{DD} applied to the depletion region is symmetrical and conductivity becomes zero, As the reverse bias voltage increases across the junction, the thickness of depletion region also increases.

When V_{DS} is applied and V_{GS}=0

- When drain voltage, the drain current I_D flows as shown in fig. this drain current causes voltage drop along the channel (this is due to n-material is resistive or drain has some internal resistance), this voltage drop reverse bias the pn junction, causes into the channel.
- And this depletion region penetrates maximum into the channel because channel is lightly doped when compared to gate.
- reverse bias is higher near drain than source hence the shape of the depletion is wedge shaped.

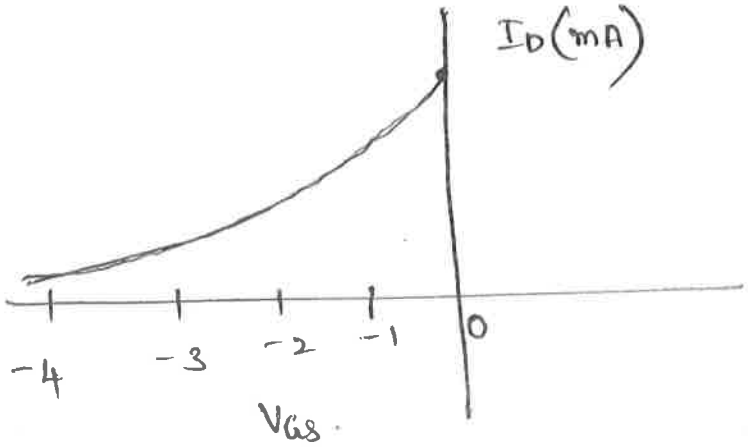
When V_{DD} and V_{GG} applied

- The drain current is maximum when no external voltage is applied between gate and source and it is I_{DSS}.
- When $V_{GG}(V_{GS})$ is increased beyond zero, the depletion regions are widened this reduces the effective width of the channel and controls the drain current through the channel.
- Whenever V_{GS} is increased further, the stage is reached at which two depletion regions touch each other, it called as "Pinch off region", this reduces drain current to zero.
- The voltage at which the drain current becomes zero is known as Pinch off voltage.
- This pinch off voltage(V_p) is negative for N-Channal JFET and it is depends on (a) doping of the N and P regions of device and (b) the width of channel.

Characteristics of JFET:

There are two important characteristics of JFET
(a) Transfer Characteristics
(b) Drain or VI Characteristics.

Transfer Characteristics:



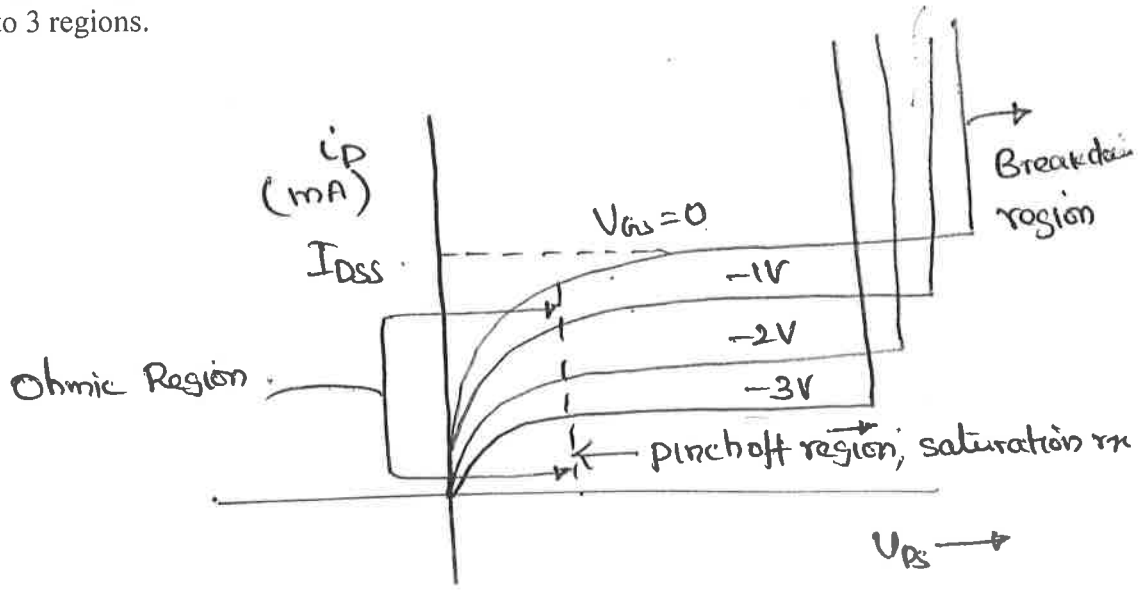
- This gives the relationship between drain current I_D and gate to source voltage(V_{GS}) for different values of V_{DS}.
- Whenever V_{GS}=0, the drain current will be the maximum i.e. I_{DSS}.
- Whenever V_{GS} increased, the depletion region maximum penetrates into the channel this causes the drain current will be zero, that voltage is known as "Pinch Off Voltage".
- The relation between I_{DSS} and pinch off voltage V_P is

The relation between I_{DSS} and V_P is

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Drain or VI Characteristics:-

- This gives the relation between V_{DS} and drain current I_D and the output characteristics are divided into 3 regions.



Ohmic Region:

- When $V_{DS}=0$ there is no attracting potential at the drain and hence drain current $I_D=0$, even channel between gates is fully open.
- As V_{DS} increased I_D increases linearly upto some point this shows that FET behave like an ordinary resistor so this resion is called as "Ohmic Region".

Pinch off region:

- When V_{DS} is increased the channel width reduced to a minimum value known as "Pinch Off" and the voltage at which "Pinch off" occurs is known as pinch off voltage.
- This region also known as saturation region or constant current region.
- In this region, drain current remains constant at its maximum value I_{DSS}.
- The relation between I_{DSS} & V_{GS} and V_P is

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

This relation is also known as shockly's equation.

Break down region:

In this region the drain current increases rapidly with increase in V_{DS}.

JFET parameters :- An important parameter of a JFET is the current I_{DSS} which is the drain saturation current when $V_{GS}=0$. Besides this there are 3 most important parameters of a JFET. They are derived from the basic equation $i_D = f(V_{gs}, V_{ds})$

a) Transconductance or Mutual conductance (g_m) :- The mutual conductance at an operating point is defined as the ratio of small change in drain current to the small change in gate voltage keeping drain voltage const

Unit is Siemens.

$$g_m = \left.\frac{\Delta i_d}{\Delta V_{gs}}\right|_{V_{ds}=\text{const}}$$

b) Dynamic drain resistance (r_d) : It is defined as the ratio of small change in drain voltage to the small change in drain current keeping gate voltage constant.

$$r_d = \left.\frac{\Delta V_{ds}}{\Delta i_d}\right|_{V_{GS}=\text{const}}$$

c) Amplification factor (μ) : It is the ratio of small change in drain voltage to the small change in gate voltage when I_D is kept constant.

$$\mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{i_D=\text{const}}$$

FET Small signal Model :-

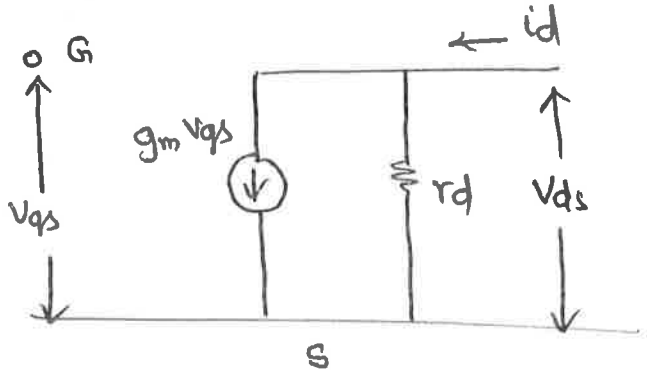
$$i_D = f(V_{GS}, V_{DS})$$

$$\Delta i_d = \left.\frac{\partial i_D}{\partial V_{GS}}\right|_{V_{DS}} \Delta V_{GS} + \left.\frac{\partial i_D}{\partial V_{DS}}\right|_{V_{GS}} \Delta V_{DS}$$

Using small signal notation

$$i_d = g_m V_{gs} + \frac{1}{r_d} V_{ds}$$

The above equation can be implemented as shown below

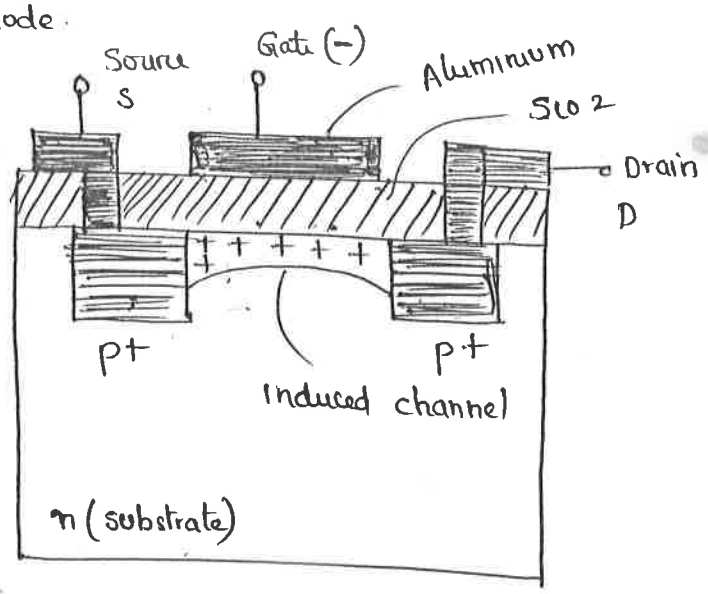


The relation between μ, g_m, r_d is given by

$$\boxed{\mu = g_m r_d}$$

The Metal oxide semi conductor FET (MOSFET)

MOSFET is also called as Insulated Gate Field Effect Transistor (IGFET). There are fundamentally two types n channel and p channel type. They can be operated in Enhancement Mode and depletion Mode.



P channel MOSFET : It consists of a highly doped n type substrate into which two highly doped p+ regions are diffused as shown in the figure. The p+ sections act as source and drain for the FET. A thin layer of SiO_2 is grown over the surface of the structure. The gate metal is over laid on the oxide layer covering the entire channel region. The contact to the metal over the channel is called as Gate terminal. Gate metal, SiO_2, channel forms like a capacitor. As the gate is insulated from the channel by SiO_2 layer it is called as IGFET. This layer results in high input resistance (10^{10} to $10^{15}\ \Omega$) for the FET.

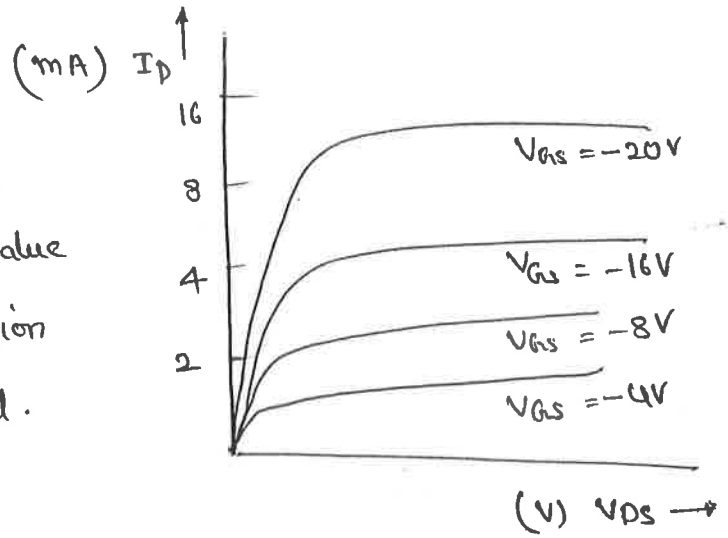
The Enhancement MOSFET :- After grounding the substrate by applying the negative voltage to the Gate, it induces positive charges towards channel. The positive charges which are minority carriers in the n type substrate form an "inversion layer." of the -ve voltage on Gate increases the induced positive charge increases. Thus the drain current is enhanced by the -ve Gate voltage and such device is called as Enhancement type MOSFET

Characteristics of MOSFET :- There are two types of characteristics. They are

a) drain characteristics (V_{DS} Vs I_D — V_{GS} const)

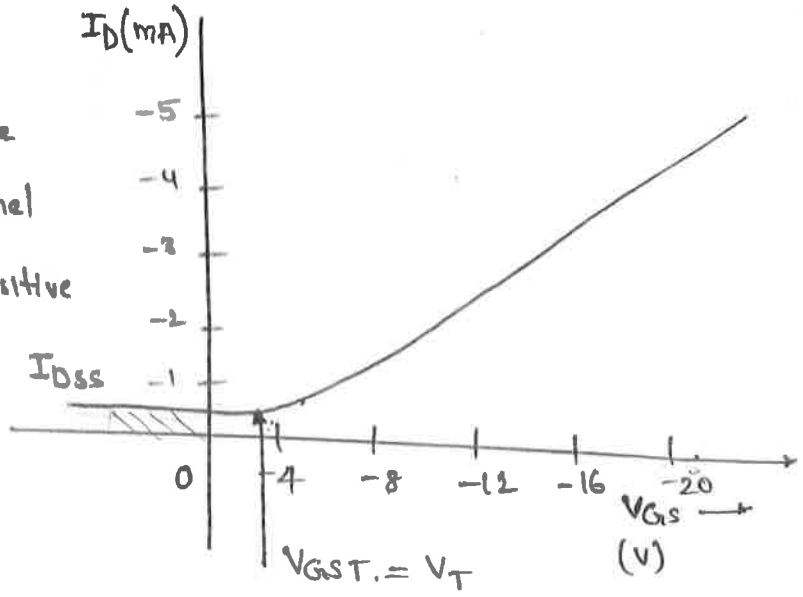
b) Transfer characteristics (V_{GS} Vs I_D — V_{DS} const)

Drain characteristics :- It is graph plotting between V_{DS} and I_D keeping V_{GS} constant. Like ordinary FET it is observed that I_D increases with V_{DS} upto some extent and it maintains constant after some value of V_{DS}. It maintains ohmic region and saturation region as usual.

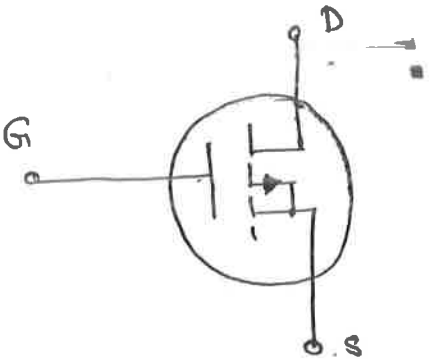


Transfer curve :

I_D increases with -ve value of V_{GS} as the induced channel increases. If V_{GS} is made positive current decreases and it finally reached to I_{DSS}.



Enhancement type MOSFET Symbolic representation :



p channel Enhancement type MOSFET.

The Depletion MOSFET : In this type of MOSFET initally a channel is diffused between the source and drain. The type of impurity used for the channel diffusion should be same as source and drain. The construction of n channel depletion type MOSFET is shown below. in fig (a)

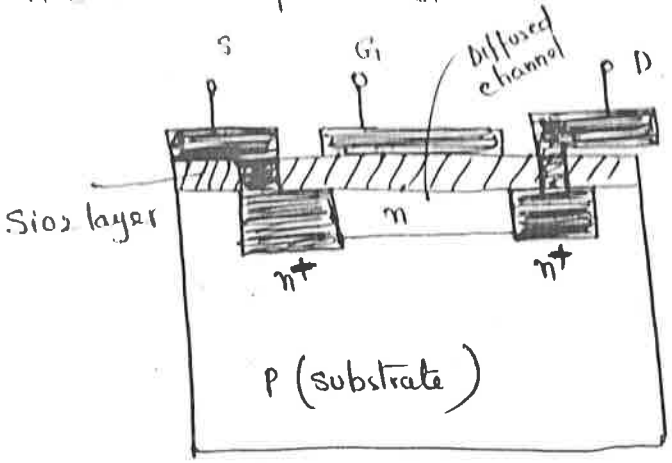


Fig (a)

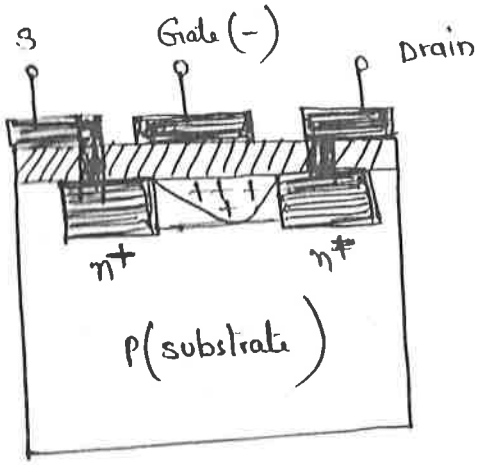
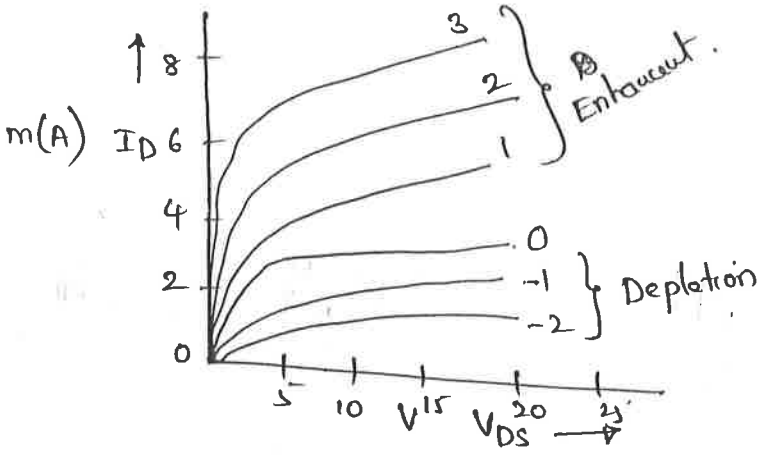


Fig (b).

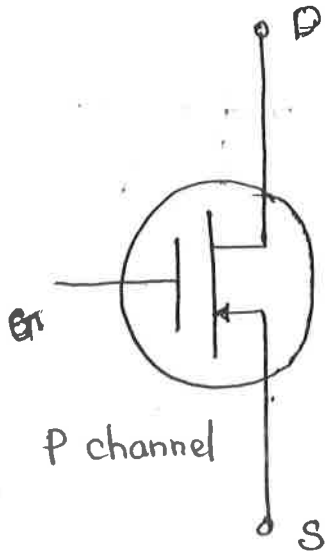
Operation :- In this type of MOSFET initally a channel is diffused between the source and drain with the same type of impurity used for source and drain. In this FET an appreciable amount of drain current flows even for $V_{GS} = 0$. If the -ve voltage on gate increases positive charges are induced on other side due to capacitive effect and making channel less conductive and the drain current decreases. The distribution of charge in the channel causes an effective depletion of Majority carriers which accounts for the name "depletion MOSFET." The shape of the depletion region is like a wedge shaped region like in ordinary FET. The VI characteristics of Depletion type MOSFET and FET are similar.

The depletion type MOSFET can be operated in both

The characteristics are given below.

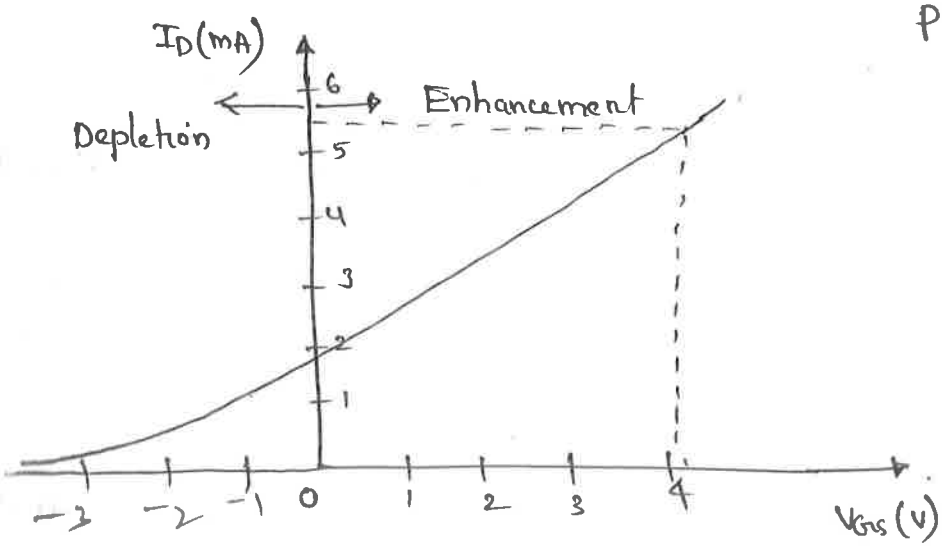


Drain characteristics.



P channel

Symbolic representation of p channel MOSFET.



Transfer Characteristics

Enhancement Mode :- In this mode, Gate Voltage made +ve hence it ve induces more negative charges and hence drain current increases. which is shown in the characteristics (I_D increases)

Depletion Mode : In this mode, Gate Voltage is -ve and induces more no positive charges and depletion of majority carriers takes place. and the drain current decreases as shown in the characteristics.

UNIT-6

Comparison of JFET and MOSFET

JFET

(a) It operates only in depletion mode because the input junction is always reverse biased.

(b) Input impedance of JFET is less because gate takes a very small leakage current.

(c) Drain resistance is high.

(d) Difficult to fabricate.

(e) PN junction formed between gate and channel.

(f) It does not requires any additional protection circuits.

MOSFET

(a) MOSFET operates in both enhancement and depletion method.

(b) MOSFET has high input impedance than JFET because the gate current is negligible.

(c) Drain resistance is less.

(d) Easier to fabricate.

(e) There is no PN junction, due to the SiO_2 layer between gate and channel it acts as capacitor.

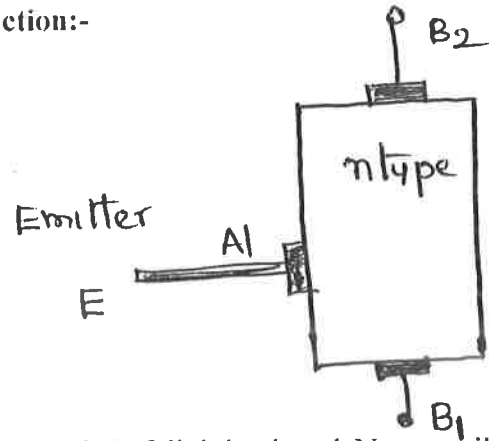
(f) MOSFET get damaged easily, if they are not operated properly thus additional protective circuits are needed.

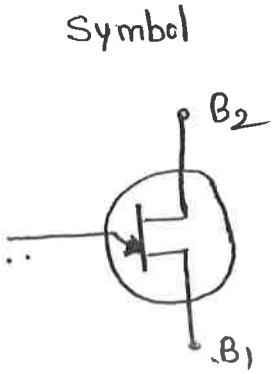
UNIT-6

UJT (Uni Junction Transistor):

- It has only one PN junction but it has a three terminal silicon diode.
- It differs from an ordinary diode in the sense that it has three leads and also it difference from BJT & FET that it has no ability to amplify.
- It has negative resistance characteristics which makes it useful as an oscillator.

Construction:-

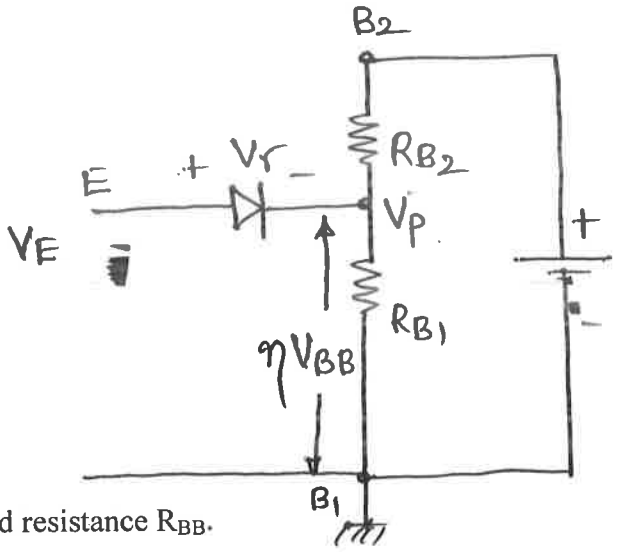




It consist of lightly doped N type silicon bar sandwiched with heavily doped P-type material for producing single PN junction.

The three terminals named as emitter E, two base terminals B2&B1 arrow points gives the direction of conventional current when UJT is in conducting state.

Equivalent circuit:



$$V_p = \frac{V_{BB}}{R_{B1}+R_{B2}} \cdot R_{B1}$$

- It consist of a diode and resistance R_{BB}.

η = Intrinsic stand off ratio

- The diode D represents PN junction and R_{BB} represents the resistance between B2&B1 or total resistance of silicon bar from one end to other with emitter terminal opens, it is called as inter base resistance.

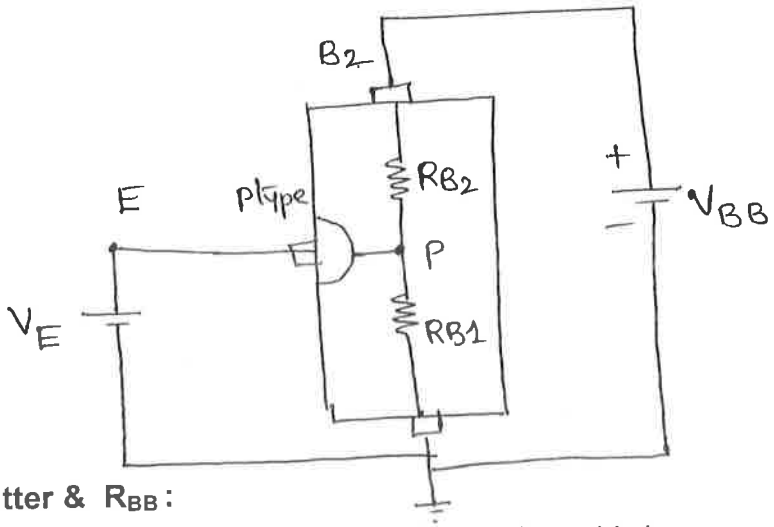
  Here

  $R_{BB} = R_{B1} + R_{B2}$

  At point A, $R_{B1} > R_{B2}$, R_{B1} = 60% of R_{BB}

  R_{B1} is variable because its value depends upon the bias voltage across PN junction.

Operation :



When voltage applied at the emitter & R_{BB} :

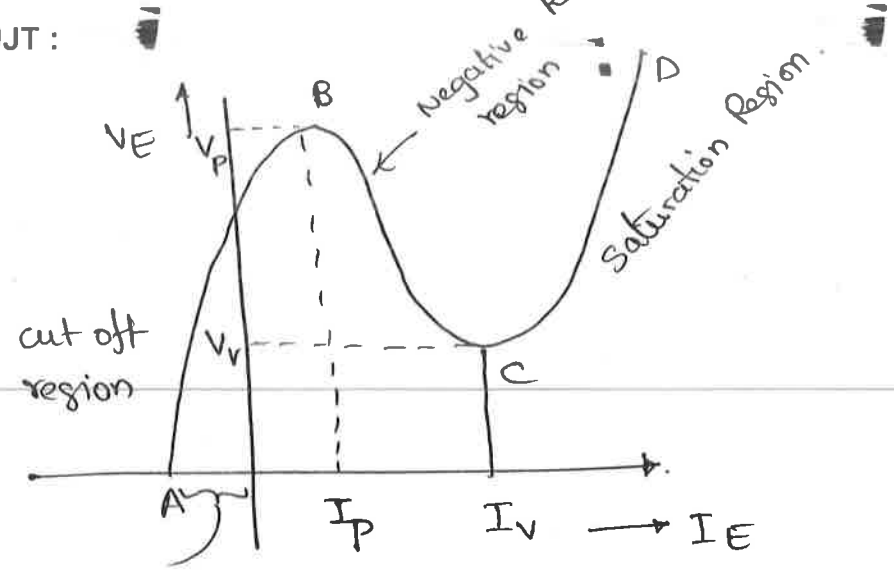
When V_{BB} is applied between B_2 and B_1 while the variable emitter voltage V_E is applied across emitter terminals.

If $V_E < \eta V_{BB} + V_r$ UJT is OFF

$V_E > \eta V_{BB} + V_r$ UJT is ON

The diode drop V_r is generally 0.3 to 0.7 V

Characteristics of UJT :



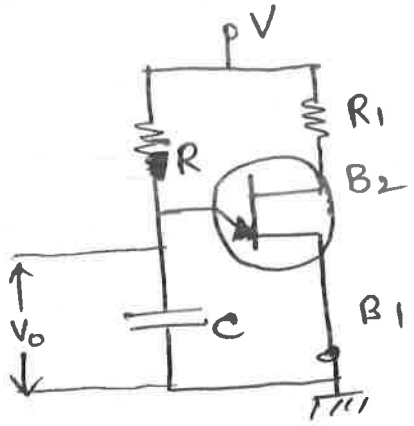
- Initially $V_E < V_P$, emitter junction is reverse biased resulting in a small emitter current flows.
- When $V_E > V_P$, emitter junction is forward biased and hence current flows through emitter this current increases until the peak current I_P reaches point P, the holes are injected into N region which are repelled by base B_2, while they are attracted by base 1. These holes increases conductivity between emitter and base 1. V_E drops and I_E increases until it reaches the valley point V_V.
- At the valley point, the current increased to such an extent that there is no further increase in conductivity thus the device behaves as a conventional forward biased PN-junction.
- Between the peak point and valley point, V_E decreases and I_E increases thus UJT shows a negative resistance between this region. After valley point UJT enters into saturation region i.e. very small change in I_E increases V_E largely.

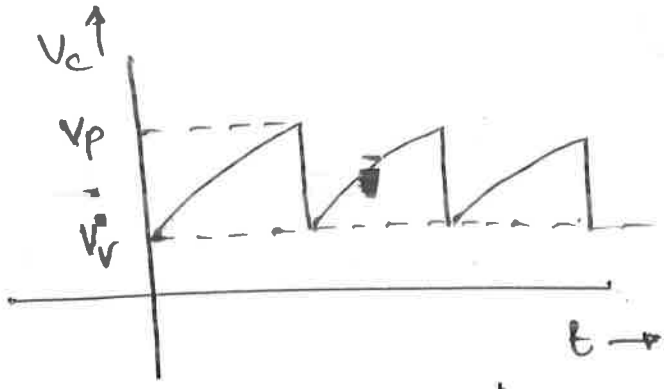
Applications of UJT:

It has a unique property, that it can be triggered by any one of its three terminal or an output can be taken from any one of its three terminals.

(a) Switching Circuits
(b) Pulse generation
(c) Saw tooth generation
(d) Timing & trigger circuits
(e) Sine Wave Generation
(f) Voltage related supplies.

UJT AS Relaxation oscillator:

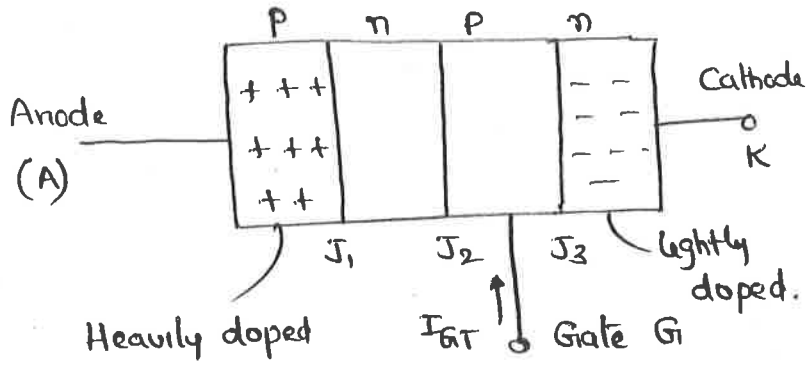




output waveform across capacitor.

- Zt consist of UJT & C which is charged through R as V_{BB} switched on.
- when capacitor voltage reaches the value V_p, in time T_s UJT fires and rapidly discharges C through B_1 till the voltage falls below minimum value V_V. The device is cut off and C starts to charge

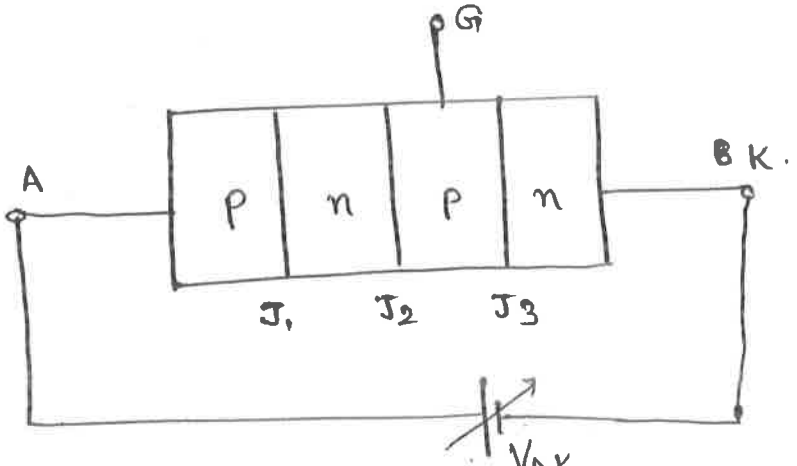
Silicon controlled Rectifier (SCR) :- The SCR is a four layer pnpn device where p and n layers are alternately interchanged. The outer layers are heavily doped. There are three pn junctions called J_1, J_2 and J_3. There are 3 terminals called as Anode, cathode and Gate. The constructional diagram is shown below.



Anode is positive with respect to the cathode. to forward bias SCR. To make SCR ON, a current is to be passed through the gate terminal I_{GT}. Thus it is a current operated device.

Operation of SCR :- Operation is devided into two catagories.

a) when Gate is open :-

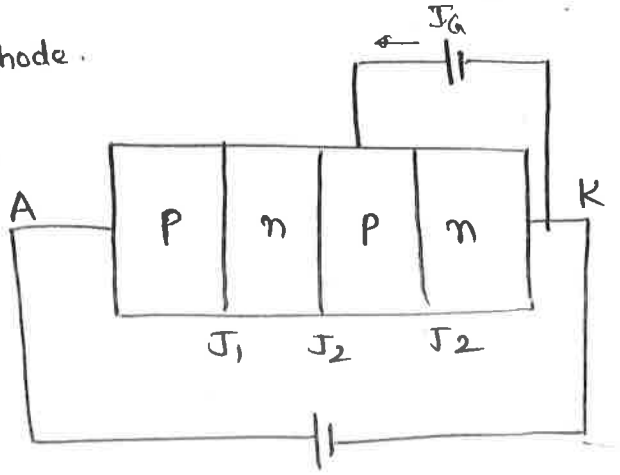


when the Anode is positive with respect to cathode and the Gate is opened, junctions J_1, J_3 are forward biased and the junction J_2 is reverse biased. Then a small leakage current flows through the junction J_2. Then SRCR is said to be in OFF state. This is called forward blocking state of SCR and the voltage applied between Anode and cathode is called forward voltage.

with gate open, of cathode is positive with respect to the anode, J_1, J_3 are reverse biased and J_2 is forward biased. Then a

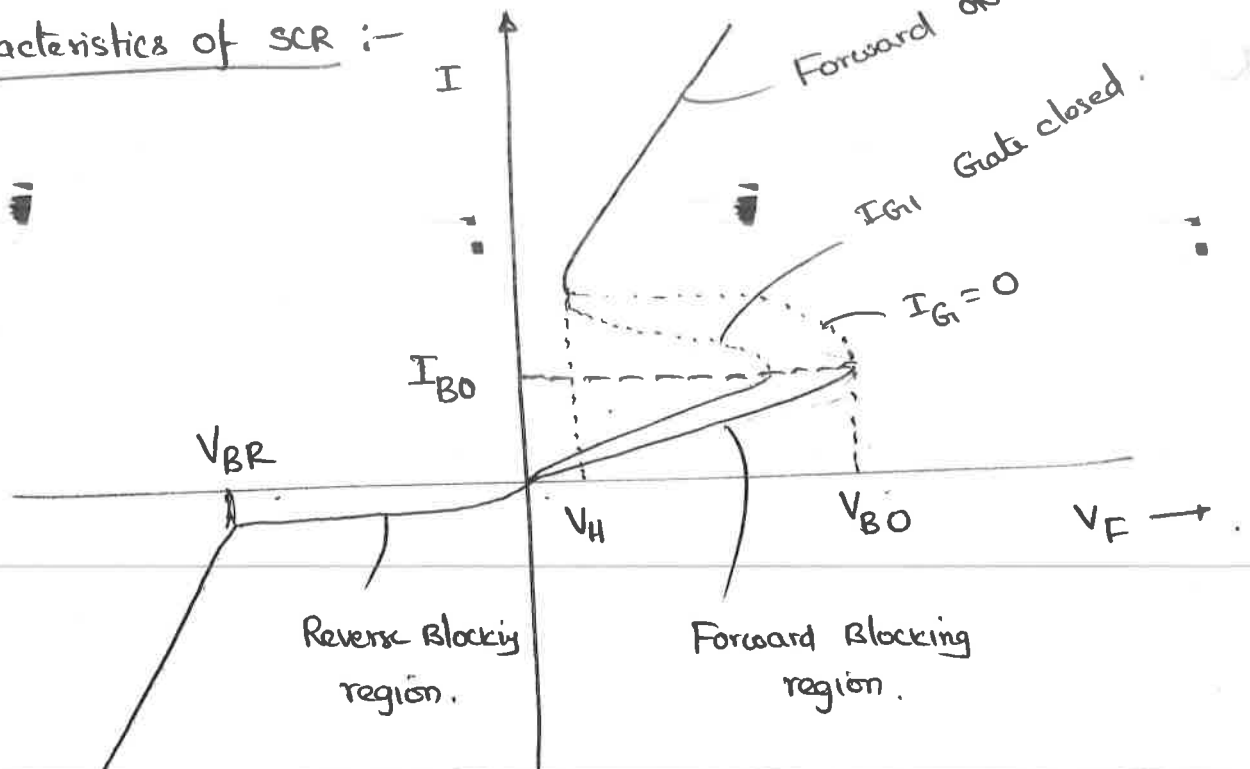
In the forward blocking state, if the voltage is increased the current is zero upto certain limit. At a particular value of voltage the junction J2 breaks and SCR conducts heavily. This is called forward breakover voltage V_{BO} of SCR. and in such condition SCR is said to be triggered.

b) when Gate is closed : consider that voltage is applied between Gate and cathode when the SCR is in forward blocking state. The gate is +ve with respect to cathode.



Along with J1 and J3 junctions J2 is also forward Biased. Then SCR conducts heavily. i.e SCR can be triggered at very low voltage of V_{AK} when a small gate voltage is applied.

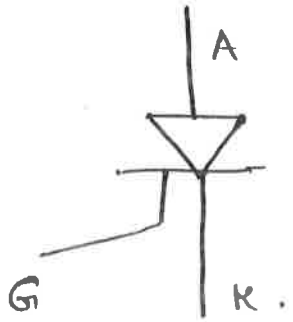
Characteristics of SCR :-



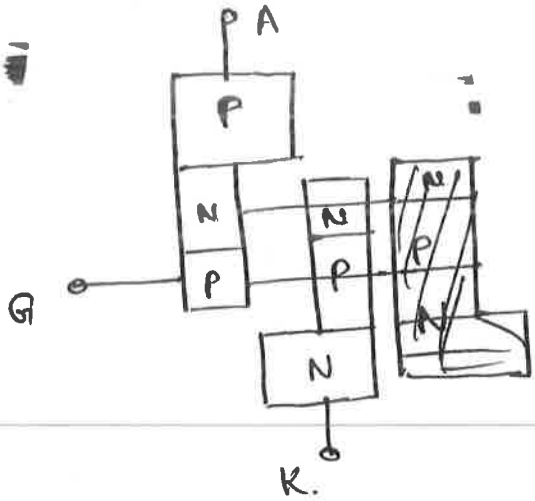
Forward characteristics :- It shows a forward blocking region when $I_G = 0$. Forward voltage increases upto V_{BO}, SCR turns ON and high current flows. It is also shown that SCR will be turned ON at lower voltage when a small voltage is applied to Gate.

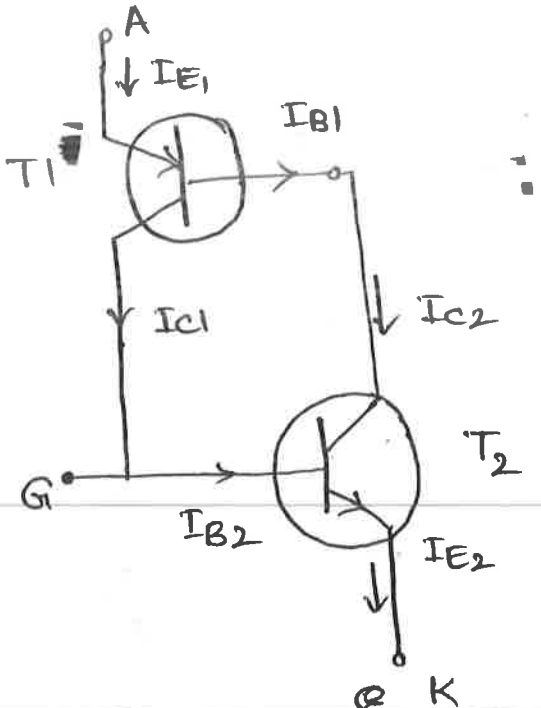
Reverse characteristics :- If the anode to cathode voltage is reversed, then the device enters into reverse blocking region. If the reverse voltage is increased a large reverse current flows due to avalanche Breakdown. This voltage is called reverse breakdown voltage.

Symbol of SCR :-



SCR Analysis using two Transistors Analogy :- SCR can be viewed as back to back connection of two transistors PNP and NPN. as shown in the figure.





The collector of T_1 becomes base of T2 and collector current of T_2 becomes base current of T_1. when the Voltage is given to Gate it forward biases the base, emitter junction of T_2 and collector current I_{C_2} increases. I_{C_2} is nothing but the base current of Transistor T1. Then Indirectly both emitter current and collector currents of T_1 increases This process is cumulative and both transistors enter into saturation, and making all the junctions forward biased. This results in large anode current.

SCR parameters :-

Holding current (I_H) :- It is the value of current below which SCR switches from conduction state to forward blocking state.

Latching current (I_L) :- This is the minimum current flowing from anode to cathode when SCR goes from OFF to ON state and remains in ON state even after gate voltage is removed. It is greater than, but very close to holding current.

—o—

Applications : Used in Fan regulation

Used to control the power to Electrical devices.

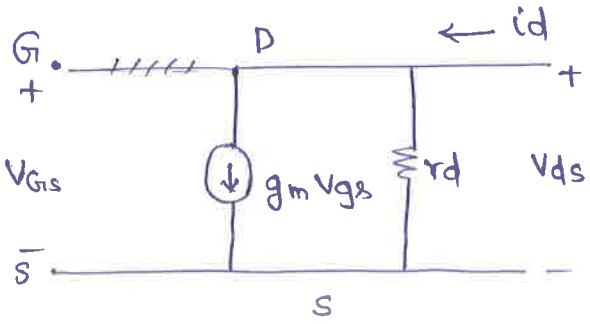
FET Analysis

$$i_D = f(V_{GS}, V_{DS})$$

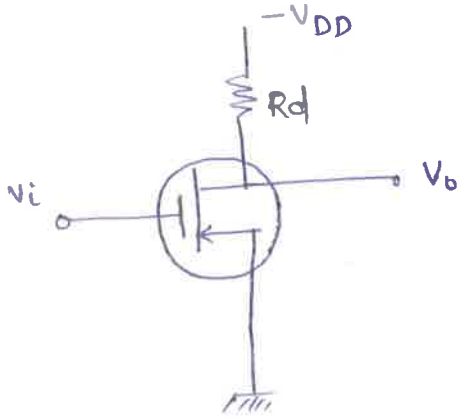
$$\Delta i_d = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}} \Delta V_{GS} + \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}} \Delta V_{DS}$$

$$\boxed{i_d = g_m V_{gs} + \frac{1}{r_d} V_{ds}} \qquad \boxed{\mu = g_m r_d}$$

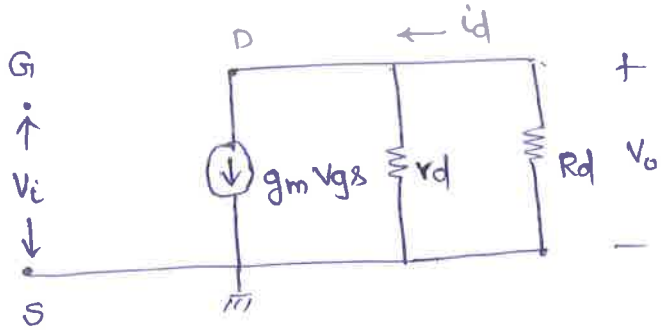
Low Frequency small signal FET Model :



Low Frequency common source Amplifier :-



Equivalent ckt :



Voltage gain $A_V = \frac{V_o}{V_i} = \frac{-i_d R_d}{V_i} = \frac{-\left(g_m V_{gs} + \frac{V_o}{r_d}\right) R_d}{V_i}$

$$A_V = -g_m R_d - \frac{R_d}{r_d} \cdot \frac{V_o}{V_i}$$

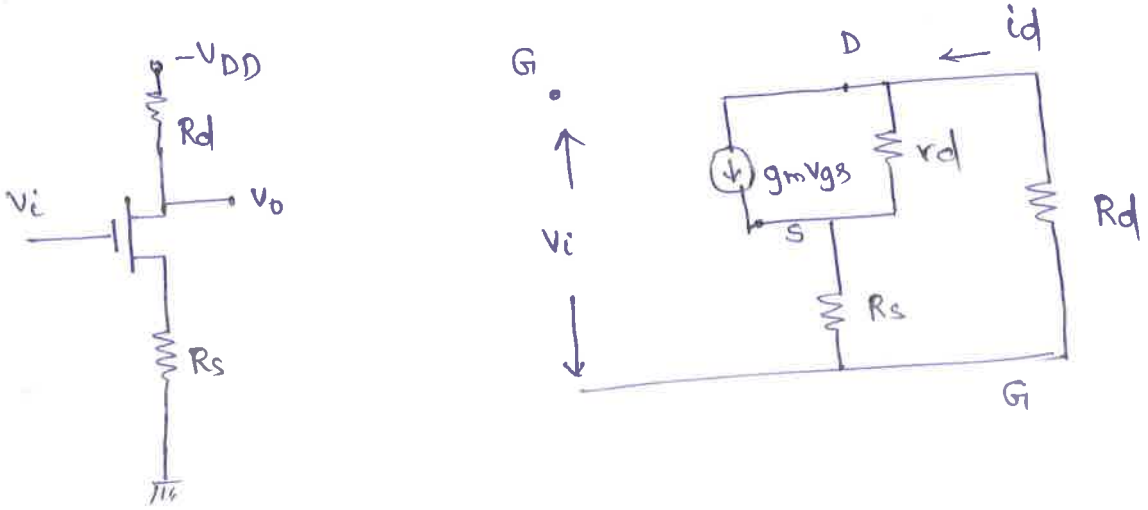
$$A_v\left(1+\frac{R_d}{r_d}\right) = -g_m R_d$$

$$A_v\left(r_d + R_d\right) = -g_m r_d R_d \qquad \text{But} \quad \mu = g_m r_d$$

$$\boxed{A_v = \frac{-\mu R_d}{r_d + R_d}}$$

Common Source Amplifier with Unbypassed Source Resistance :-

Equivalent ckt :-



Applying KVL to o/p ckt :

$$i_d R_d + (i_d - g_m V_{gs}) r_d + i_d R_s = 0$$

$$i_d R_d + i_d r_d + i_d R_s = g_m r_d V_{gs}$$

$$i_d\left(r_d + R_d + R_s\right) = \mu V_{gs}$$

$$i_d = \frac{\mu V_{gs}}{r_d + R_d + R_s} \qquad V_{gs} = V_i - i_d R_s$$

$$i_d = \frac{\mu V_{gs}\left(V_i - i_d R_s\right)}{r_d + R_d + R_s}$$

$$i_d r_d + i_d R_d + i_d R_s + \mu R_s i_d = \mu V_i$$

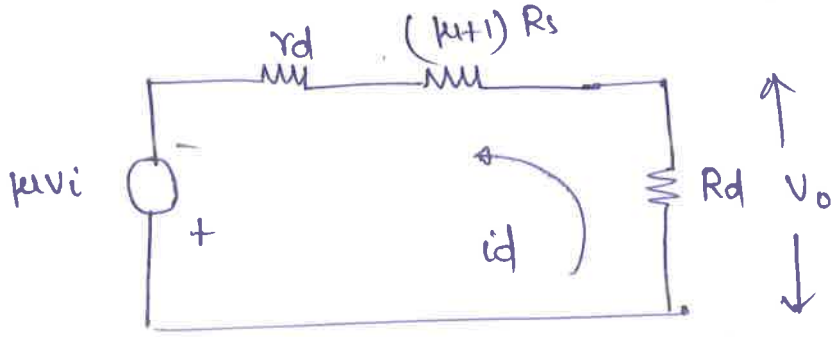
$$i_d = \frac{\mu v_i}{r_d + R_d + (\mu+1) R_s}$$

$$V_o = -i_d R_d$$

$$V_o = \frac{-\mu v_i R_d}{r_d + R_d + (\mu+1) R_s}$$

$$\boxed{\frac{V_o}{V_i} = \frac{-\mu R_d}{r_d + R_d + (\mu+1) R_s}}$$

The above equation can be written as



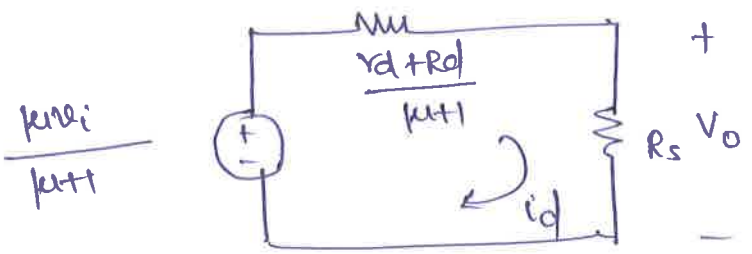
Common Drain Amplifier : From the above ckt

$$V_o = i_d R_s$$

$$V_o = \frac{\mu v_i \cdot R_s}{r_d + R_d + (\mu+1) R_s}$$

$$= \frac{\mu v_i / (\mu+1) R_s}{\frac{r_d + R_d}{\mu+1} + R_s}$$

The equivalent ckt is

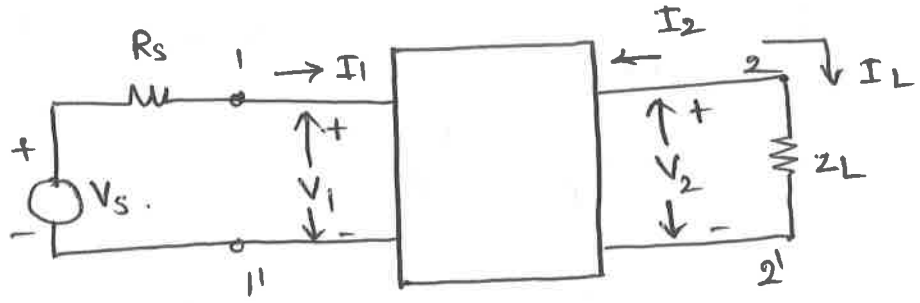


If $R_d = 0$, $(\mu+1) R_s \gg r_d$

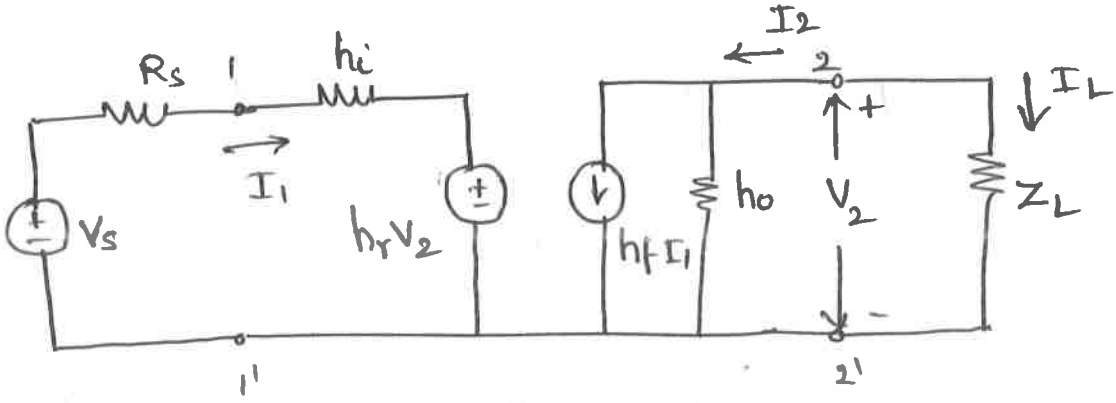
$$A = \frac{\mu R_s}{(\mu+1) R_s} \qquad \mu \gg 1$$

$\therefore A = 1$ Source follower.

Analysis of a Transistor Amplifier using h parameters :-



converting the above ckt into h parameter Model we have



current gain :- $A_I = \frac{I_L}{I_1} = \frac{-I_2}{I_1} = -\left(\frac{h_f I_1 + h_o V_2}{I_1}\right)$

$$A_I = -h_f + h_o \cdot \frac{V_2}{I_1} = -h_f + h_o \cdot \frac{-I_2 Z_L}{I_1}$$

$$A_I (1 + h_o Z_L) = -h_f$$

$$\boxed{A_I = \frac{-h_f}{1 + h_o Z_L}}$$

Input Impedance (Z_i) :- $Z_i = \frac{V_1}{I_1} = \frac{h_i I_1 + h_r V_2}{I_1}$

$$= h_i + h_r \cdot \frac{(-I_2 Z_L)}{I_1} = h_i + h_r \cdot A_I Z_L$$

$$\therefore \boxed{Z_i = h_i + h_r A_I Z_L}$$

Voltage gain or Voltage Amplification (A_V) :-

$$A_V = \frac{V_2}{V_1} = \frac{-I_2 \cdot Z_L}{V_1} = \frac{A_I I_1 Z_L}{V_1} = \frac{A_I I_1 Z_L}{I_1 Z_i} = A_I \frac{Z_L}{Z_i}$$

$$\boxed{A_V = A_I \cdot \frac{Z_L}{Z_i}}$$

Voltage gain Taking source Resistance into Account : (A_{VS})

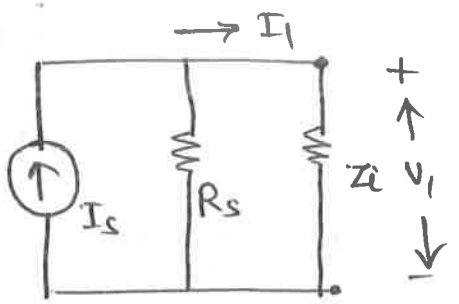
$$A_{VS} = \frac{V_2}{V_S} = \frac{V_2}{V_1} \cdot \frac{V_1}{V_S} = A_V \cdot \frac{V_1}{V_S}$$

From the circuit $V_1 = \frac{V_S \cdot Z_i}{Z_i + R_S}$ $\therefore \frac{V_1}{V_S} = \frac{Z_i}{Z_i + R_S}$

$$\boxed{A_{VS} = A_V \cdot \frac{Z_i}{Z_i + R_S}}$$ If $R_S = 0$ $\boxed{A_{VS} = A_V}$

Current gain Taking Source Resistance into account : (A_{IS})

$$A_{IS} = \frac{-I_2}{I_S} = \frac{-I_2}{I_1} \cdot \frac{I_1}{I_S} = A_I \cdot \frac{I_1}{I_S}$$



For the above ckt

$$I_1 = \frac{I_S \cdot R_S}{Z_i + R_S} \cdot \frac{I_1}{I_S} = \frac{R_S}{Z_i + R_S}$$

$$\boxed{A_{IS} = \frac{A_I \cdot R_S}{Z_i + R_S}}$$

The output Admittance : (Y_o)

$$Y_o = \left.\frac{I_2}{V_2}\right|_{V_s=0} \quad \text{and} \quad R_L = \infty$$

$$Y_o = \frac{h_f I_1 + h_o \cdot V_2}{V_2} = \frac{h_f I_1}{V_2} + h_o$$

with $V_s = 0$ from the input ckt we have

$$(h_i + R_s) I_1 + h_r V_2 = 0$$

$$(h_i + R_s) I_1 = -h_r V_2$$

$$\frac{I_1}{V_2} = \frac{-h_r}{h_i + R_s}$$

$$\therefore Y_o = h_o - \frac{h_f h_r}{h_i + R_s}$$

Summary : The generalized equations are

$$A_I = \frac{-h_f}{1 + h_o Z_L} \qquad A_{Is} = \frac{A_I \cdot R_s}{Z_i + R_s}$$

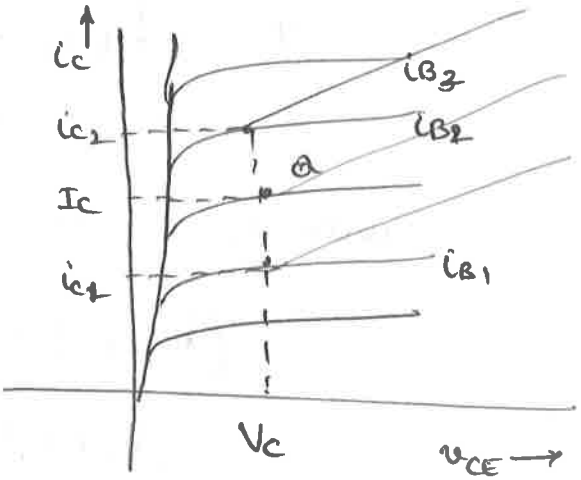
$$Z_i = h_i + h_r A_I Z_L$$

$$A_V = A_I \frac{Z_L}{Z_i} \qquad A_{Vs} = \frac{A_V \cdot Z_i}{Z_i + R_s}$$

$$Y_o = h_o - \frac{h_f h_r}{h_i + R_s}.$$

Evaluation of h parameters from characteristics :- There are four h parameters hie, hre, hfe, hoe for common emitter configuration. hie and hre will be obtained from input characteristics and hfe, hoe are from output characteristics.

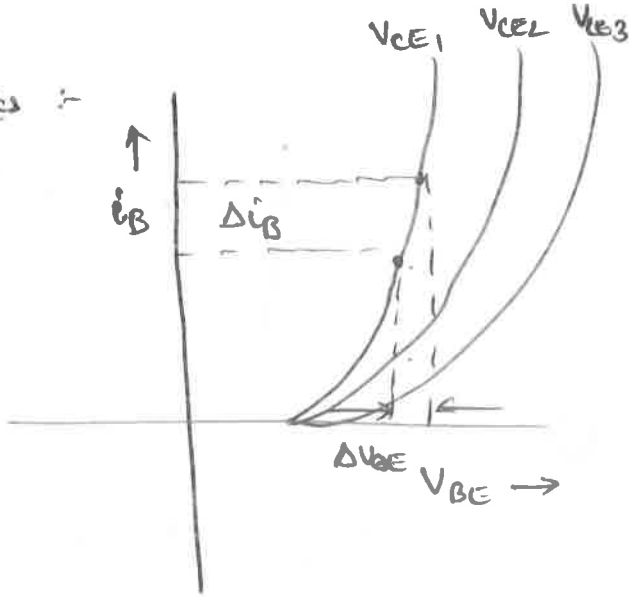
hfe and hoe from o/p characteristics:



$$h_{fe} = \frac{\partial i_C}{\partial i_B} = \frac{\Delta i_C}{\Delta i_B}\Big|_{V_{CE}=\text{const.}}$$

$$h_{oe} = \frac{\partial i_C}{\partial V_{CE}}\Big|_{i_B=\text{constant}}$$

hie and hre from i/p characteristics :-



$$h_{ie} = \frac{\Delta V_{BE}}{\Delta i_B}\Big|_{V_{CE}=\text{const}}$$

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}\Big|_{i_B=\text{const.}}$$

———— o ————

Common Collector configuration : (Emitter Follower) :-

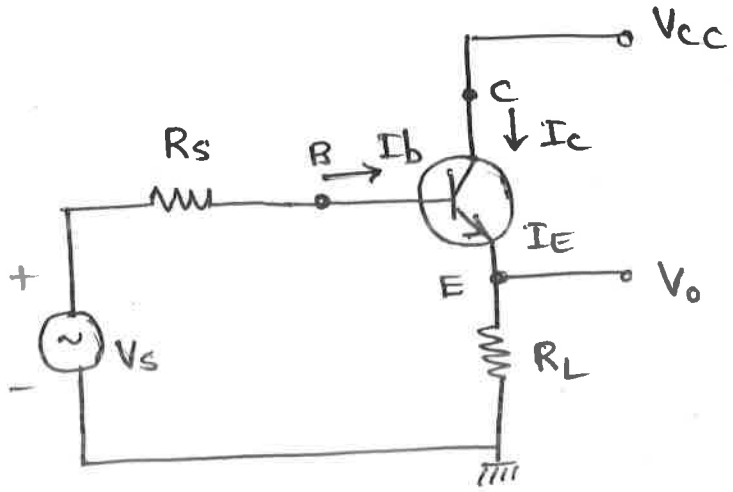
As the emitter follows input signal it is called as emitter follower

The voltage gain is unity for emitter follower.

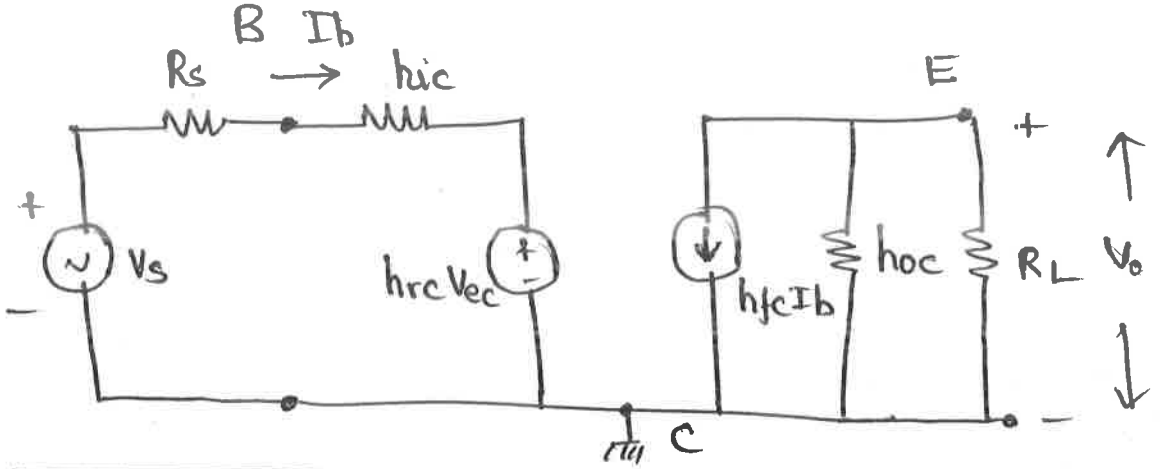
Features of CC or Emitter follower :

1) Voltage gain is unity
2) R_i is very high
3) R_o is very low
4) Used as buffer circuit.
5) It increases power level of signal.

The circuit is shown below :



The h parameter equivalent ckt :-



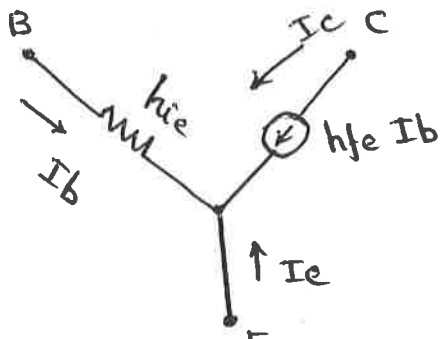
$$A_I = \frac{-h_{fc}}{1 + h_{oc} R_L}$$

$$A_V = \frac{A_I R_L}{R_i}$$

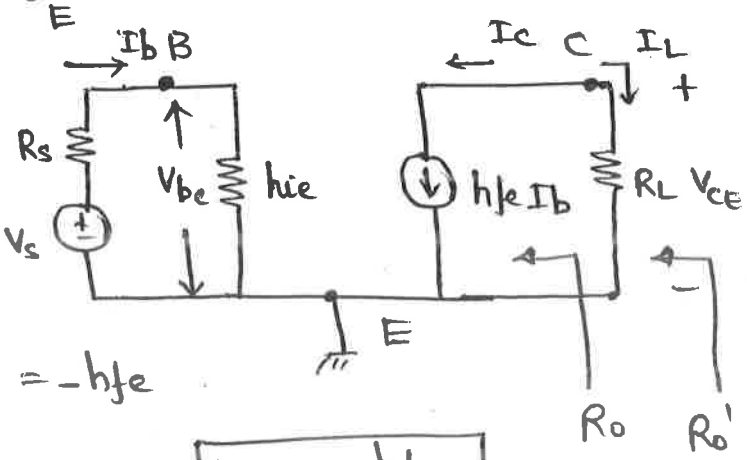
$$R_i = h_{ic} + h_{rc} A_I R_L$$

$$Y_o = h_{oc} - \frac{h_{fc} h_{rc}}{h_{ic} + R_s}$$

Simplified Hybrid Model :- This analysis will be used whenever hoe $R_L < 0.1$. In this analysis hie, hfe are sufficient. The following approximate hybrid model may be used for all three configurations.



Approximate CE Model :-



a) current gain A_I :

$$A_I = \frac{-I_c}{I_b} = \frac{-h_{fe} I_b}{I_b} = -h_{fe}$$

$$\therefore \boxed{A_I = -h_{fe}}$$

b) Input Impedance : Z_i or R_i

$$R_i = h_{ie} + h_{re} A_I R_L \approx h_{ie}$$

$$\boxed{R_i = h_{ie}}$$

(or) $\frac{V_{be}}{i_b} = h_{ie}$

c) Voltage gain A_V : $A_V = \frac{V_{ce}}{V_{be}} = \frac{-I_c R_L}{h_{ie} I_b} = \frac{A_I \cdot R_L}{h_{ie}}$

$$\therefore \boxed{A_V = \frac{-h_{fe} R_L}{h_{ie}}}$$

d) output Impedance : $R_o = \frac{1}{Y_o}$

$$R_o = \left.\frac{V_{ce}}{I_c}\right|_{V_s = 0} \quad \text{(or)} \quad Y_o = \left.\frac{I_c}{V_{ce}}\right|_{V_s = 0}$$

$Y_o = \frac{h_{fe} I_b}{V_{ce}}$ From i/p ckt $i_b(R_s + h_{ie}) = 0$

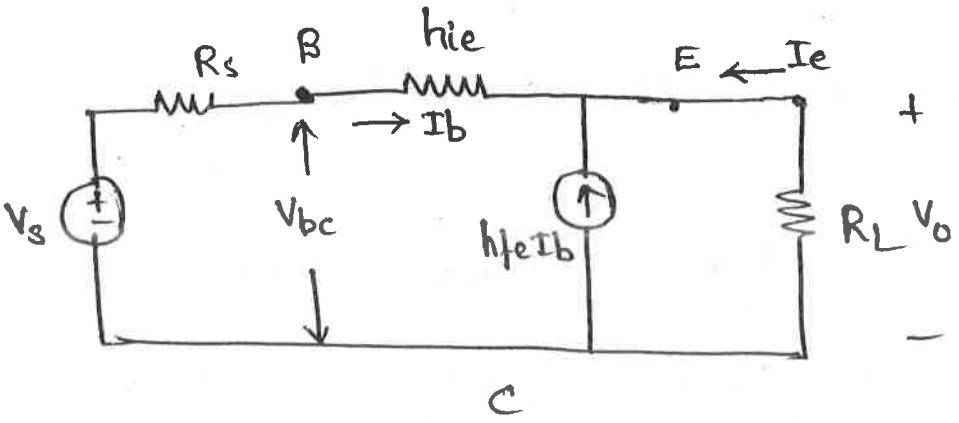
$\therefore i_b = 0$

$Y_o = 0 \quad \therefore \quad R_o = \frac{1}{0} = \infty.$ $\boxed{R_o = \infty}$

$R_o' = R_o \parallel R_L = \infty \parallel R_L = R_L$

$\boxed{R_o' = R_L}$

Emitter Follower using Simplified hybrid Model :-



$A_I = \frac{-I_e}{I_b} = \frac{+(I_b + h_{fe} I_b)}{I_b} = +(1 + h_{fe})$

$R_i = \frac{V_{bc}}{I_b} = h_{ie} + \frac{R_L(1+h_{fe}) I_b}{I_b} = h_{ie} + (1+h_{fe}) R_L$

$A_V = \frac{A_I \cdot R_L}{R_i} = \frac{(1+h_{fe}) R_L}{h_{ie} + (1+h_{fe}) R_L} = \frac{R_i - h_{ie}}{R_i}$

$= 1 - \frac{h_{ie}}{R_i}$

$R_o = \frac{R_s + h_{ie}}{1 + h_{fe}}$

$R_o' = R_o \parallel R_L$

Conversion Formulae :-

$$h_{ic} = h_{ie} \quad h_{rc} = 1 \quad h_{fc} = -(1+h_{fe}) \quad h_{oc} = h_{oe}$$

$$h_{ib} = \frac{h_{ie}}{1+h_{fe}} \qquad h_{rb} = \frac{h_{ie}h_{oe}}{1+h_{fe}} - h_{re}$$

$$h_{fb} = \frac{-h_{fe}}{1+h_{fe}} \qquad h_{ob} = \frac{h_{oe}}{1+h_{fe}}$$

Comparision of Transistor configurations :-

	CE	CC	CB
A_I	High	High	Low
h_i	1100 Ω	1100 Ω	21.6 Ω
A_V	High	Low	High
h_r	2.5×10^{-4}	≈ 1	2.9×10^{-4}
R_i	Medium	High	Low
h_f	50	-51	-0.98
R_o	Medium	Low	High
h_o	25 μA/V	25 μA/V	0.49 μA/V

Use of h parameters :-

1. They are real Numbers at Audio Freqvencies
2. Easy to Measure
3. They can be obtained from Transistor characteristics
4. Convinient to use in circuit Analysis and design
5. Most of the Manufacturers specify h-parameters